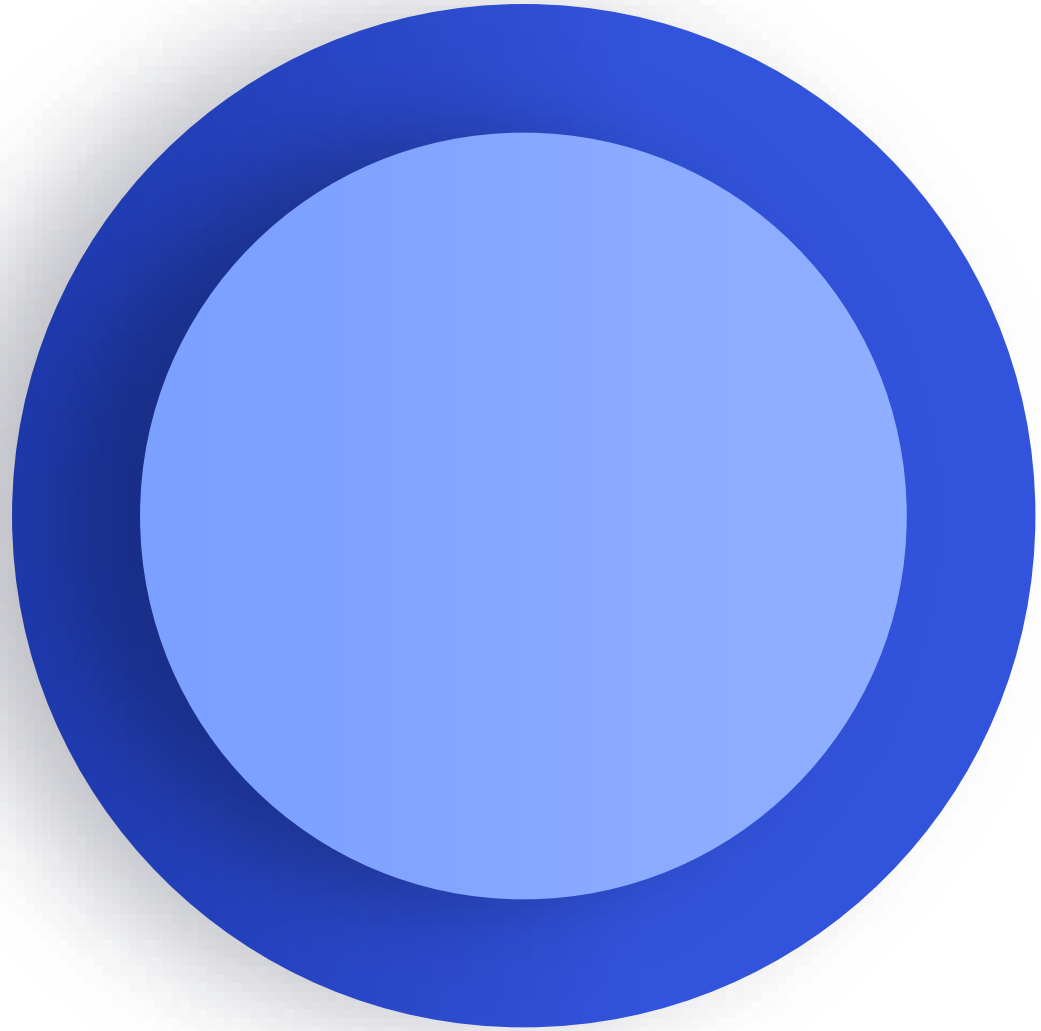
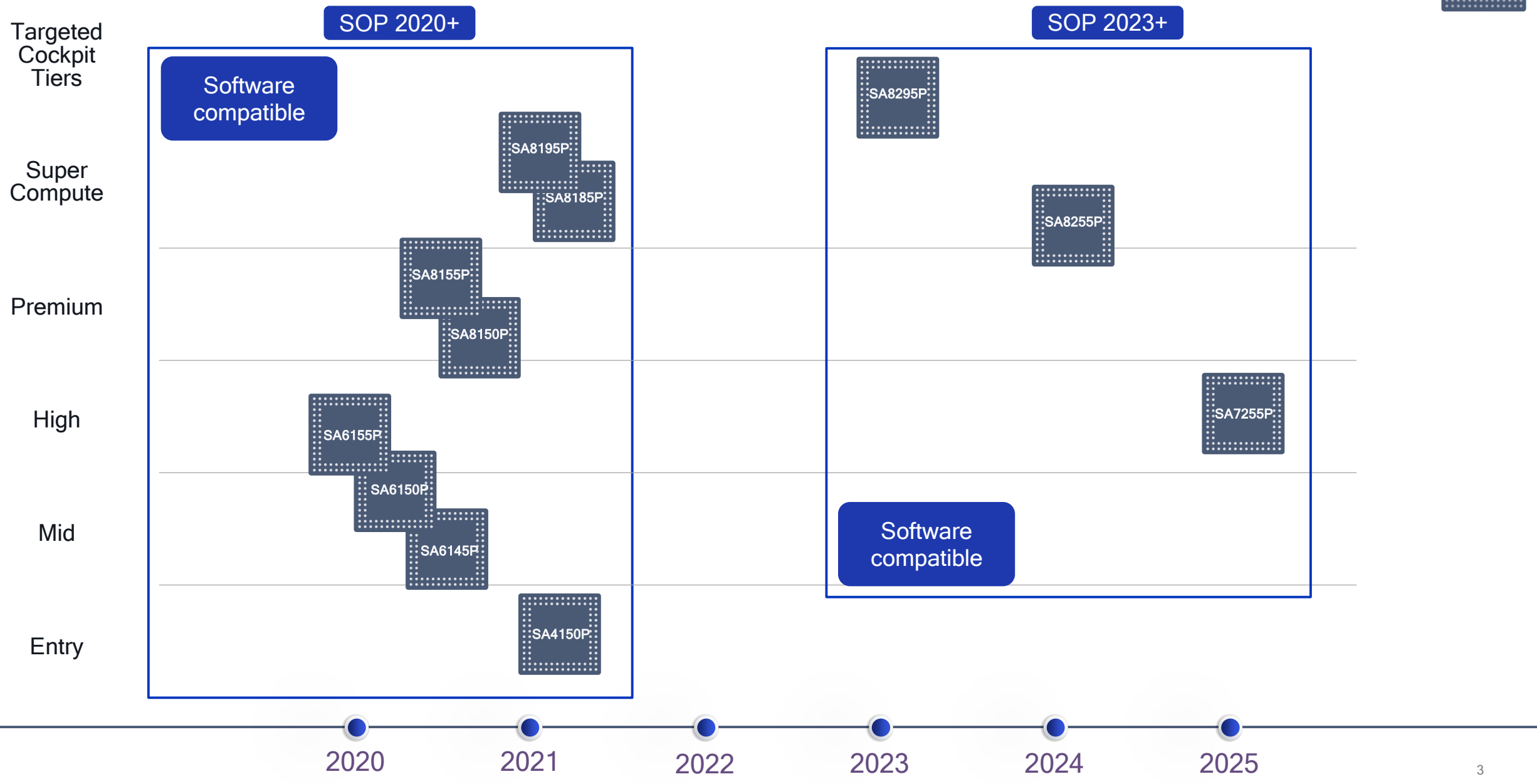
Qualcomm® Automotive SOCs SA7255P product proposal

Compute Roadmap



Qualcomm Automotive Infotainment Roadmap



SA7255P product highlights

Qualcomm’s next generation IVI MID SoC

- Targeting Mid Integrated Cockpit and Infotainment Applications
  - HW & SW support for multi-OS domains driving multi-displays up to 4k60
  - Pre-integrated Linux and Hypervisor with RTOS and Android VMs, including auto enhancements
- Scalability with High-end SA8255P and Premium SA8295P series
  - Common platform that harmonizes certain building blocks including GPU and HW Virtualization
  - Single Software product for all Gen4 SOCs can be supported
  - SoftSKU with over-the-air upgrade support using Car-to-Cloud services
- Lower system BOM compared to previous generation
  - Integrated ISP to process up to 6x 2Mpix 24bit HDR bayer sensors, RGB-IR HW support
  - Integrated CAN-FD bus controllers
  - Integrated AV1 HW video decoder
- ASIL-B compliant
  - ASIL-B compliant processing chain for RVC/AVM/DMS/eMirror (including CSI input, ISP, CPU and GPU)
- AEC-Q100 grade 3 qualified
- Cost effective attach chips for Power Management, Connectivity and GNSS

Qualcomm Automotive compute SKUs

* With external SERDES (Superframe over DSI, 2x/4x Superframe over DP MST)
**- DMIPS is not an estimate of true performance. Estimated only
*** - HMX- Hexagon Matrix eXtension

(subject to change)

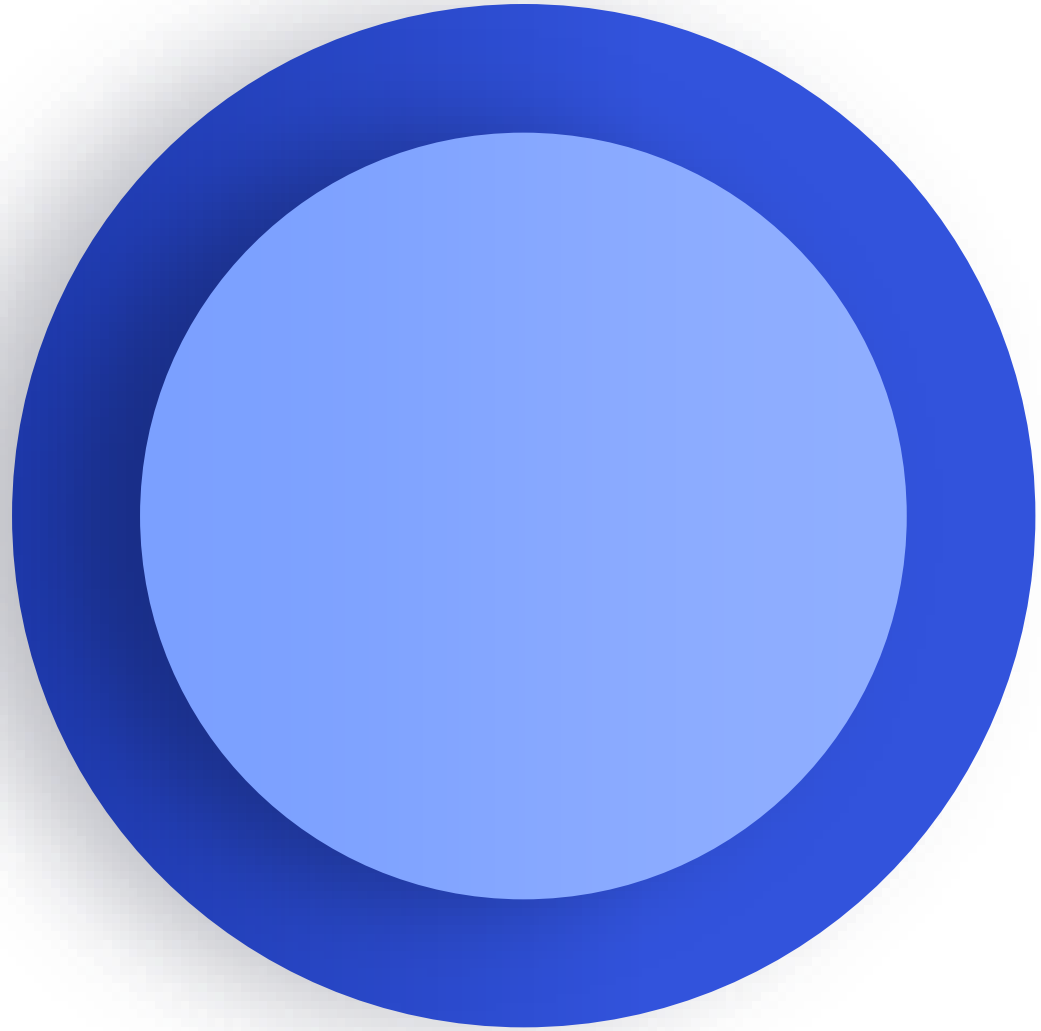
Chipsets	SA8295P-BAAA SiP only	SA8255P-AAAA SiP only	SA7255P-AAAA	SA8195P	SA8155P	SA6155P
CPU	Octa Core Kryo Gen6	Octa Core Kryo Gen6	Octa Core Kryo Gen6	Octa Core Kryo Gen 4	Octa Core Kryo Gen 4	Octa Core Kryo Gen 4
DMIPS*	185K	185K	100K	96K	77K	50K
DMIPS with compiler optimizations*	230K	230K	126K	120k	98k	64K
GFLOPS (16b/32b)	2.9 TFLOPS (32)/ 5.8 TFLOPS (16) 245fps Man3.0	1.3 TFLOPS (32)/ 2.6 TFLOPS (16) 195fps Man3.0	420 GFLOPS (32)/ 840 GFLOPS (16) 68fps Man3.0	2.1 TFLOPS (32)/ 4.2 TFLOPS (16) 184fps Man3.0	1.0 TFLOPS (32)/ 2.0 TFLOPS (16) 113fps Man3.0	110 GFLOPS (32)/ 220 GFLOPS (16) 14fps Man3.0
Memory	8x16 LPDDR4x @ 2133 MHz	6x16 LPDDR5 @ 3200 MHz	4x16 LPDDR5/5x @ 3200 MHz	8x16 LPDDR4x @ 2133 MHz	4x16 LPDDR4x @ 2133 MHz	2x16 LPDDR4x @ 1555 MHz
Bandwidth (With UBWC)	>200 GB/s (incl. x3 gain)	>240 GB/s (incl. x3 gain)	150 GB/s (incl. x3 gain)	204 GB/s (incl. x3 gain)	102 GB/s (incl. x3 gain)	26 GB/s (incl. x2 gain)
Addressable Memory	Up to 32 GB with inline ECC	Up to 36 GB with inline ECC	Up to 32 GB with inline ECC	Up to 32 GB	Up to 16 GB	Up to 8 GB
Audio DSP (LPASS)	Q6 DSP @ 1.5 GHz	Q6 DSP @ 1.5 GHz	Q6 DSP @ 1.5 GHz	Q6 DSP @ 1.5 GHz	Q6 DSP @ 1.5 GHz	Q6 DSP @ 1.0 GHz
Compute DSP + HTA	Q6 DSP with 4xHVX + HMX*** ~46 TOPS for 8-bit FP	Q6 DSP with 4xHVX + HMX ~24 TOPS for 8-bit FP	Q6 DSP with 4xHVX + HMX ~10 TOPS for 8-bit FP	Optional: Q6 DSP with 4x HVX @ 1.5 GHz + HTA @ 900 MHz	Optional: Q6 DSP with 4x HVX @1.5 GHz + HTA @ 900 MHz	Optional: Q6 DSP with 2x HVX @ 1.1 GHz
# of Concurrent Displays*	Up to 32	Up to 28	Up to 10	Up to 12	Up to 8	Up to 6
Display Interfaces	2x DSI 6x DP, 2x eDP,	2x DSI 4x DP	1x DSI (4-lanes), 1x DP1.4 (4-MST)	2x DSI (both 4-lanes), 3x DP 1.4, 1x eDP 1.4	2x DSI (4-lanes), 1x DP1.4	1x DSI (4-lanes), 1x DP1.4 (2-MST)
Typ. Pixel/Resolution Supported	Typical 64 Mpix - 6x4k	Typical 48 Mpix - 5x4k	Typical 12 Mpix - 1x4K + 2x1920x1080	Typical 30 Mpix - 3x4k or 6x2880x1080	Typical 24 Mpix - 3x4K or 4x2880x1080	Typical 5 Mpix - 2x1080p + 1280x720
Typ. Video Decode/Encode	4k240/4k120	4k240/4k120	4k120/4k60	4k120/4k60	4k120/4k60	4k60/1080p60

Qualcomm Automotive compute SKUs

Chipsets	SA8295P-AAAA SiP only	SA8255P-AAAA SiP only	SA7255P-AAAA	SA8195P	SA8155P	SA6155P
Camera	Up to 16 cameras 4x CSI2 4-lane	Up to 16 cameras 4x CSI2 4-lane	Up to 12 cameras 3x CSI2 4-lane	Up to 16 cameras 4x 4-lane CSI-2 v1.3	Up to 14 cameras 4x 4-lane CSI-2 v1.3	Up to 10 cameras 3x 4-lane CSI-2 v1.3
Auto Peripherals	4x PCIe Ports - 1x4+2x2+1x1 (Gen3) 2x 1GbE w/ TSN (2 x RGMII) 1x QSPI	2x PCIe Ports - 1x2 + 1x4 (Gen4) 2x 2.5 GbE w/ TSN (2 x SGMII) 1x QSPI	2x PCIe Ports - 1x2 + 1x4 (Gen4) 1x 2.5 GbE (1x SGMII) 1x QSPI	1x 4-lane PCIe 3 (RC/EP) 2x 2-lane PCIe 3 (RC) 1x 1-lane PCIe 3 (RC) 1x GbE (RGMII/RMII), 1x QSPI	1x 2-lane PCIe 3 (RC/EP) 1x 1-lane PCIe 3 (RC) 1x GbE (RGMII/RMII), 1x QSPI	1x 1-lane PCIe 2.0 (RC/EP), 1x GbE (RGMII/RMII), 1x QSPI
USB Support	4 concurrent ports - 3 xUSB 3.1 4xUSB 2.0	3 concurrent ports 2x USB 3.1 1x USB 3.0 3 USB2.0	1x USB3.1 Gen1, 1x USB2.0	2x USB3.1 Gen2 w/ DP, 2x USB3.1 Gen2	1x USB3.1 Gen2 w/ DP, 1x USB3.1 Gen2	1x USB3.1 Gen1, 1x USB2.0
Storage	2x UFS 3.1 G4 2lanes, 1x SDIO NVMe over PCIe	2x UFS 3.1 G4 2lanes, 1x 8-bit SDCC5, NVMe over PCIe	1x UFS 3.1 G4 2lanes, 1x 8-bit SDCC5, 1x eMMC 5.1	2x UFS2.1 Gear 3, 1x SD3.0, 1x NVMe over PCIe	1x 2-lane UFS3.0 Gear 4, 1x SD3.0, 1x NVMe over PCIe	1x UFS2.1 Gear 3, 1x SD3.0, 1x eMMC 5.1
Audio Support	7xTDM/I2S + 3x High Speed I2S for Radio Front-end	7xTDM/I2S + 3x High Speed I2S for Radio Front-end	7xTDM/I2S + 3x High Speed I2S for Radio Front-end	5x TDM/I2S (4x 2data lanes, 1x 4 data lanes), 2x SLIMBus, 3x High Speed I2S for Radio Front-end	5x TDM/I2S (4x 2data lanes, 1x 4 data lanes), 2x SLIMBus, 3x High Speed I2S for Radio Front-end	5x TDM/I2S (4x 2data lanes, 1x 4 data lanes), 1x SLIMBus, 2x High Speed I2S for Radio Front-end
Other Peripherals	32x Serial Interfaces, up to 228 GPIOs	25x Serial Interfaces, up to 150 GPIOs	16x Serial interfaces, up to (tbc) GPIOs	26x Serial Interfaces, up to 190 GPIOs	26x Serial Interfaces, up to 174 GPIOs	14x Serial interfaces, up to 155 GPIOs
Power Management	4x PMM8295AU	PMM8250AU + 3x PMM8251AU	2x PMM7255AU	3x PMM8195AU	2x PMM8155AU	1x PMM6155AU
Safety support	ASIL-B SAIL	ASIL-B SAIL w/ 8x CAN FD + 1x 1GbE (1x RGMII)	ASIL-B SAIL w/ 4x CAN FD + 1x 1GbE (1x RGMII)	ASIL-A, system level ASIL-B	ASIL-A, system level ASIL-B	system level ASIL-A & ASIL-B
Qualification	AEC-Q100 level 3	AEC-Q100 level 3	AEC-Q100 level 3	AEC-Q100 level 3	AEC-Q100 level 3	AEC-Q100 level 3

(subject to change)

SA7255P Overview



SA7255P product specification

Feature Set	Sub-Sets	SA7255P-AAAA (ASIL-B)
Qualcomm® Kryo™ CPU	Architecture	Octa Core
	Cores	2xA78 Prime 32/32/256 + 2xA78 Prime 32/32/256 + 4xA55 32/126, 1MB + 1MB + 512k L3
	CPU Performance	105k DMIPS
	CPU Performance with compiler optimizations*	126k DMIPS
Safety Island (SAIL)	MCU	4x Cortex R52 (lock-step or split mode), 3MB (boot memory), 1x RGMII, 4x CAN, 68 GPIOs, ASIL-B
Memory	Architecture	4x 16-bit LPDDR5 3200MHz, up to 32 GB 1 MB Sys Cache, > 150GB/s peak BW (based on UWBC) w/ ECC
GPU, Video & Display	GPU**	Adreno 621 3D core, UBWC 3.0 420GFLOPS 32-bit instructions/sec 840GFLOPS 16-bit instructions/sec (68fps Manhattan 3.0 FHD offscreen)
	APIs	OpenGL ES 3.2, Vulkan 1.2, OpenCL 2.0, C2D, ASTC
	Video Dec	4k 120fps: H.264, H.265, VP9 & AV1
	Video Enc	4k 60fps: H.264, H.265
	Video Dec + Enc	4k 60fps Dec + 4k 30fps Enc
	Display Resolutions	Typ. 12Mpix, i.e.: 1x4k @ 60fps + 2x 1920x1080 @ 60fps (FHD)
	Display Interfaces	1x 4-lane MIPI DSI 1x DP 4MST (4 streams supported)
Camera	Camera Lanes	3x 4-lane MIPI CSI-2 v1.3 (D-PHY 1.2, C-PHY 1.0)
	ISP	24bit pipeline, 2xIFE (with RGB-IR support) + 5xIFE_lite + 2xSFE_lite +1xICP + 1xIPE
AI	Neural Processor	Neural Signal Processor combo of Q6 DSP with 4xHVX + HMX (Hexagon Matrix eXtension)
	Deep Learning/AI TOPS (NSP only)	~10 TOPS for 8-bit fixed point
DSP	Audio DSP (aDSP)	Hexagon QDSP6 v66K @ xxGHz, 2 Cluster, 4 Threads (562 MPPS); 1 MB L2$ + 1 MB TCM
	General purpose DSP (gpDSP)	Hexagon QDSP6 v73M @ 1.7GHz, 2 Cluster, 6 Threads (710 MPPS); 1MB L2$

*- DMIPS is not an estimate of true performance. Estimated only with inline and optimized compiler option
**- GFLOPS is not an estimate of true performance. Turbo mode for GPU assumed. Sustained GFLOPS will be lower

SA7255P product specification

Feature Set	Sub-Sets	SA7255P-AAAA (ASIL-B)
I/O Interfaces	ETH AVB	1x 2.5 GbE (1x SGMII) supporting 8x Tx / 8x Rx dedicated virtualized channels
	PCIe	1x 2-lane and 1x 4-lane PCIe Gen4 (both RC + EP)
	USB	1x USB3.1 Gen1 1x USB2.0
	Audio Interfaces	Up to 8x I2S/PCM/TDM (3 ports are mux'ed with HS I2S)
	Secure Digital Interfaces	1x UFS 3.1 G4 2-lanes 1x 8-bit SDCC5 1x eMMC 5.1 1x OSPI / QSPI for SAIL boot
	Software Defined Radio	3x HS I2S (all ports mux'ed low speed I2S audio interfaces)
	Multiport SPI / I2C / UART	Up to 16x 4-wire QUPv3 (UART, I2C, SPI)
	GPIOs	133 GPIOs in main domain
Security		Secure boot, TrustZone® and I/O virtualization, Secure code signing, Secure memory, Secure execution environment, Secure debug, Crypto engine, Fuse array, HDCP, DTCP, User authentication
Functional safety	SOC HW	ASIL-B
Temperature		Tj max = 115°C
Package	Balls, dimensions	25x25, xx pin, 0.65mm pitch
PMIC	Balls, dimensions	9.3x9.3,181 pin, 0.65mm pitch 19 x 19 array, 45-degree ball pattern
Optional Features & Attach Chips		
Optional Low latency DSP	General purpose DSP (gpDSP)	Hexagon QDSP6 v73H @ 1.7GHz, 2 Cluster, 6 Threads (710 MPPS) 1MB L2$
Optional OTA performance upgrade	Performance	SoftSKU support
Optional Connectivity	WLAN / BT	External BT/Wi-Fi via PCIe Up to 802.11 ax DBS and BT5.x
	GNSS	External GNSS

Cockpit Soft SKUs
Life-time upgradability using Car-to-Cloud

ADAS SoC | **Cockpit SoC** | Fusion SOC

SA7255P-xxxx variants

SA7255P	X	X	X	X
	CPU*	GPU**	ML / AI	Display
A	126k	420 GFLOPS	10 TOPS	12 MP
B	96k	300 GFLOPS	5 TOPS	10 MP

SoftSKU definitions are preliminary and subject to change

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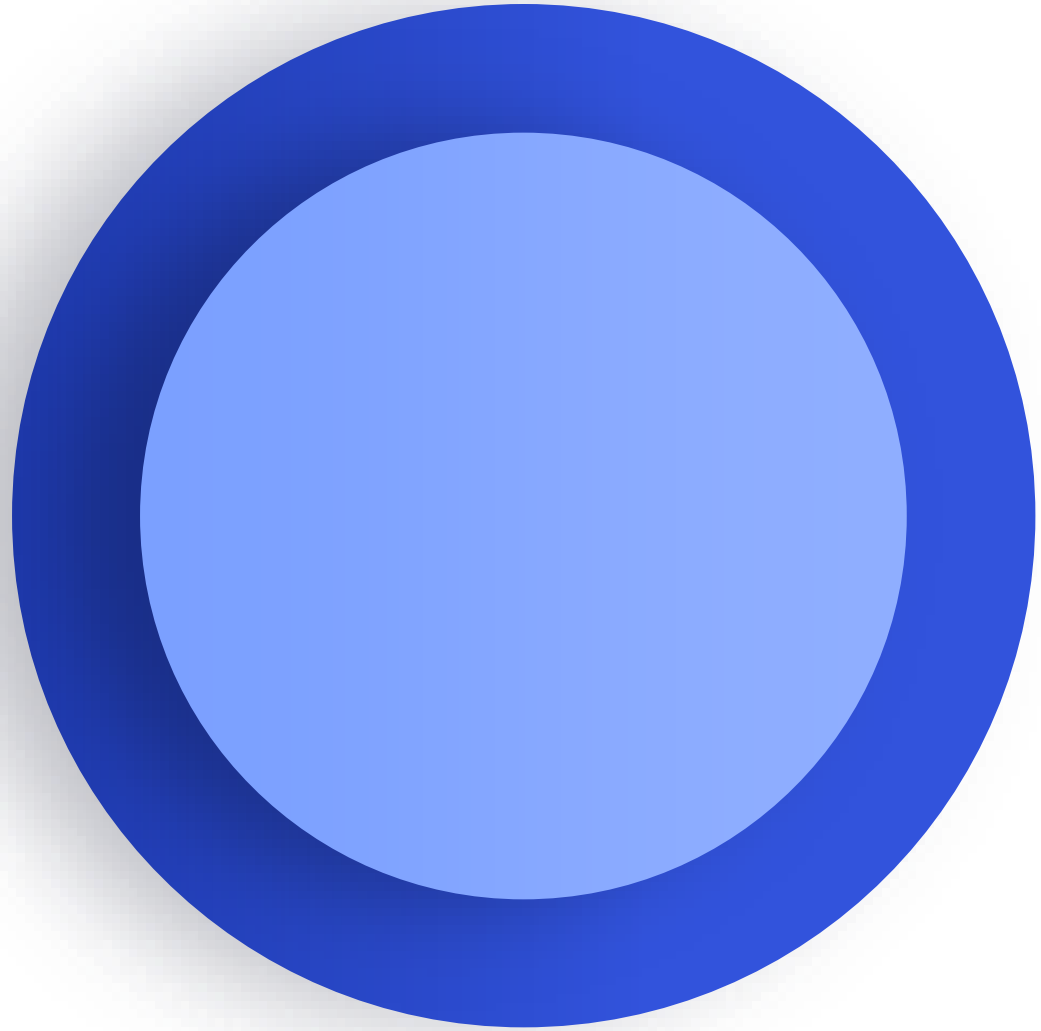
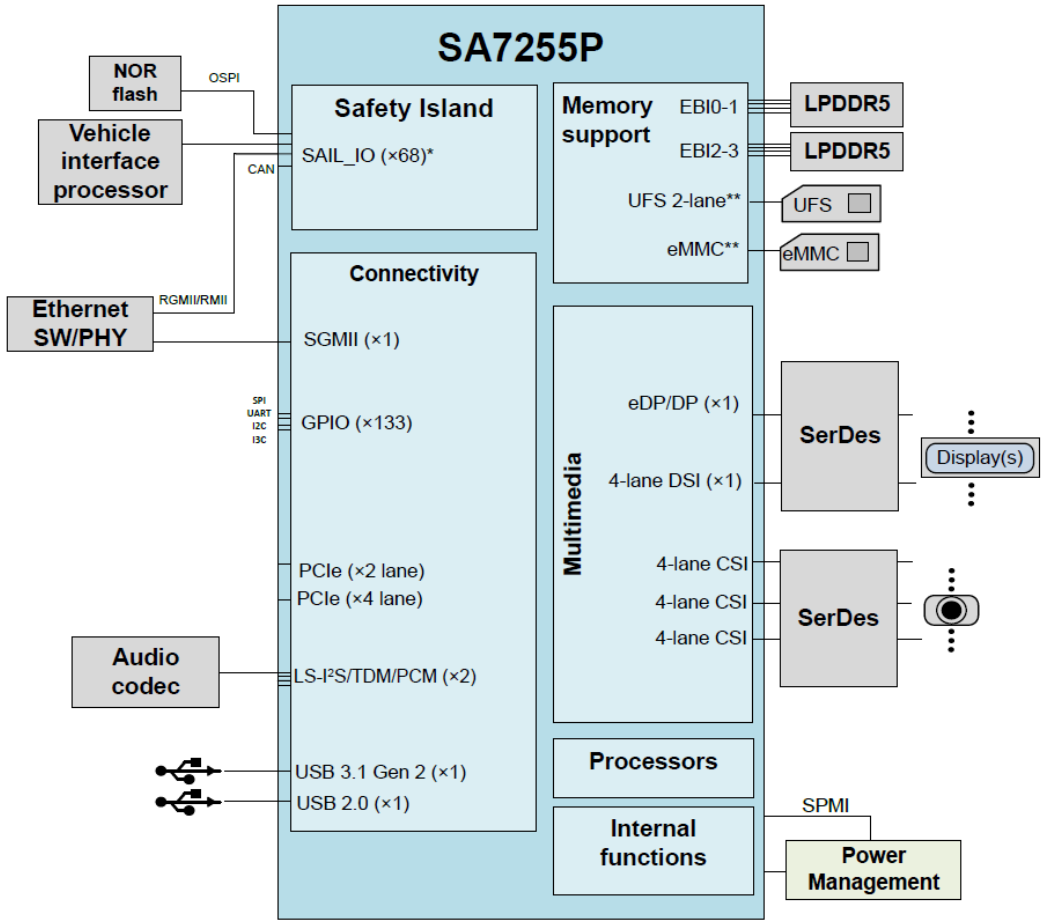
Hardware



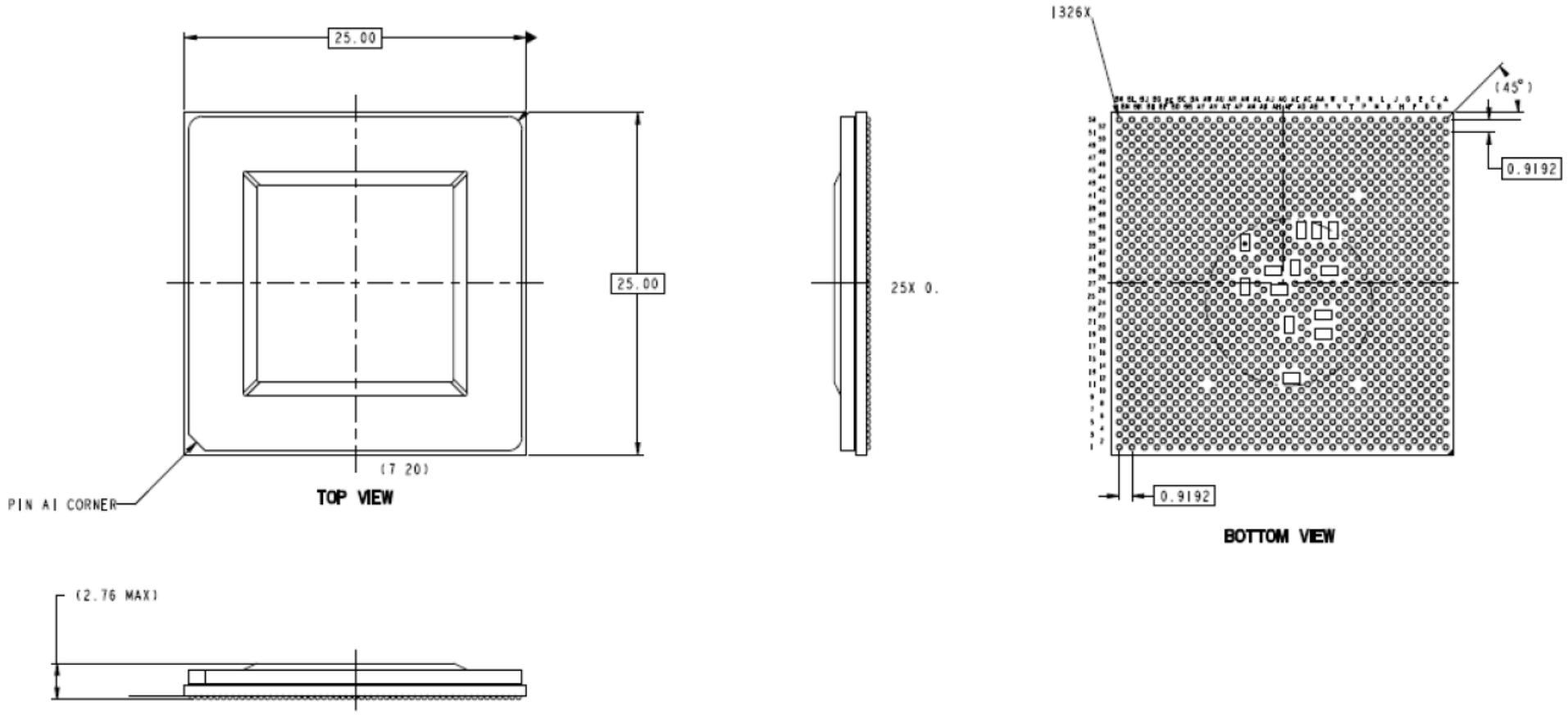
Block diagram



*Only 67 SAIL_IOs are available. SAIL_IO_52 is for internal usage only.
**eMMC and UFS cannot co-exist, either eMMC or UFS can be used.

Package

FCBGA1326+HS (Package Outline Drawing NT90-31845-1)



SA7255P HW Schedule

Preliminary information – subject to change

Milestone	Schedule
Peliminary documentation (design spec, package, schematic)	January 2023
SA7255P ES COB (chip-on-board)	August 2023
SA7255P PAPP intend sample (final HW)	February 2024
SA7255P CS COB	November 2024
SA7255P PPAP	November 2024
SA7255P OEM SOP	2025

*SIP version not planned

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Thank you!

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