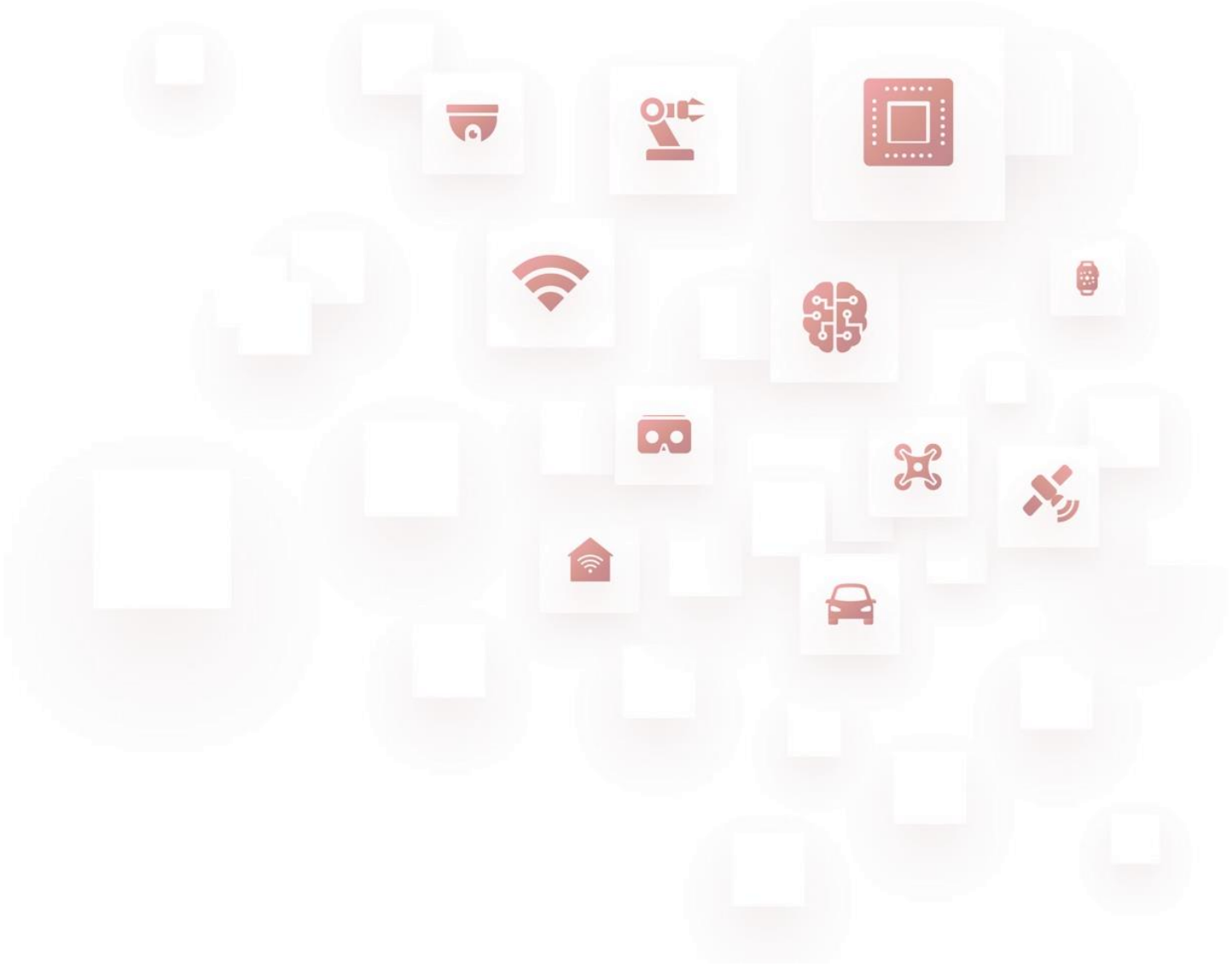
Thundercomm
AIOT ENABLER



Thundercomm TurboX C5165N SOM

Datasheet

Rev. V1.0
Aug 11, 2022

DN: tc-c-13110

Revision History

Revision	Date	Description
1.0	Aug 11, 2022	Preliminary version.

Table List

About This Document

- Illustrations in this documentation might look different from your product.
- Depending on the model, some optional accessories, features, and software programs might not be available on your device.
- Depending on the version of operating systems and programs, some user interface instructions might not be applicable to your device.
- Documentation content is subject to change without notice. Thundercomm makes constant improvements on the documentation of your computer, including this guidebook.

Table of Contents

Chapter 1. Introduction

Thundercomm TurboX C5165N System on Module (SOM) is a high-performance intelligent module, based on Qualcomm QRB5165N processor, designed with the 7 nm process, for superior performance and power efficiency with non-package-on-package (non-PoP) for better thermal dissipation.

C5165N SOM reserves interface for long range Wi-Fi, Wi-Fi 6 (Wi-Fi 802.11 a/b/g/n/ac/ax) and BT5.1. It supports two 4-lane MIPI DSI interfaces with one 5040 x 2160@60Hz or two 2560 x2560@120FPS*, support six 4-lane MIPI CSI interfaces with up to 12 cameras with 7 concurrent*, integrates multiple audio and video input/output interfaces. It provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, it supports SOM common standard protocol interfaces such as USB3.1, PCIE2.1/3.0 and I2S.

*: Depends on software variant. Camera concurrency also depends on camera parameter.

C5165N SOM provides convenient and stable system solution for IOT field, it can be embedded into the device on VR/AR, Robot, Smart Camera, AI devices, and any other connecting fields.

➲ **NOTE:** "TurboX" referred to herein is the English text of our registered trademark TURBOX.

1.1. Key features

The following table shows the detailed features of QRB5165N and C5165N SOM.

Table 1-1.Key features and performance of QRB5165N

Item	Description
Applications Processor	Kryo 585-64-bit applications processor with a 4MB L3 cache • Quad high-performance Kryo Gold cores, 3 Gold cores Fmax at 2.419 GHz, one Gold prime Fmax at 2.842 GHz • Quad low-power Kryo Silver cores, Fmax at 1.805 GHz.
Digital signal processing	Compute Hexagon DSP with quad Hexagon Vector eXtensions (quad-HVX) and Hexagon Co-processor (Hexagon CP) 2.0 Audio Hexagon DSP dedicated to audio subsystem Sensor Hexagon DSP in the Qualcomm All-Ways Aware Hub to support always-on, low-power use cases All Hexagon DSP are cache-based processors with full access to DDR
Graphics	• Adreno GPU 650 - 4K 60 FPS UI or 2x 2k 60 FPS UI • OpenGL ES 3.2, Vulkan 1.1, DX12 FL 12_1 • OpenCL 2.0 full profile
Display support	2x 4-lane DSI D-PHY 1.2 and DisplayPort 1.4 data concurrency over USB Maximum concurrency configurations • 5040 × 2160 at 60 Hz (or 120 Hz in VR mode), up to 30 bpp • Two 2560 × 2560 1 at 120 Hz for dual-panel VR displays, up to 30 bpp 4096 buffer width, and 16 hardware-layer composition
Video Encode	4K120/8K30 encode for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs
Video Decode	4K240/8K30 decode for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs
Camera support	Qualcomm Spectra 480 Camera ISP Support 6x 4 Lane MIPI CSI 64 MP 30 FPS ZSL with a dual ISP

Table 1-2.Key features and performance of TurboX C5165N SOM

Item	Description
Processor	Snapdragon™ QRB5165N
Memory	LPDDR5: 2x 4GB UFS: I/F reserved for external UFS
Connectivity	I/F reserved for external WIFI, default QCA6391
Display Interface	2x MIPI-DSI 4-lane, 5040 x 2160@60FPS
Camera Interface	6x 4 data lane MIPI CSI
Audio Interface (multiplexing with other functions)	• SoundWire interface for Qualcomm codec • SoundWire interface for Qualcomm smart speaker amplifier • 5x MI2S with 2 data lanes to support full duplex stereo • 1x MI2S with 4 data lanes for up to eight channels • DMIC ports support up to 6x DMICs
USB	1x USB 3.1 GEN2 Type-C w/ DP1.4, 1x USB3.1 gen2
PCIe	2x 2-lane PCIe Gen3, 1x 1-lane PCIe Gen3
Other Interfaces	• 1x SDC for SD card • 14x QUPs (each QUP can be set as 4-Pin SPI or 2-Pin I2C) • 4x camera dedicated I2Cs
Operating Environment	• Operation Temperature: -25°C ~ 75°C • Operation Humidity: 5%~95%, non-condensing
Power supply	3.4~4.35V, Typ. 3.8V
Dimensions	54mm x 45mm x 3.8mm
RoHS	All hardware components are fully compliant with EU RoHS 2.0 directive.

1.2. Hardware block diagram

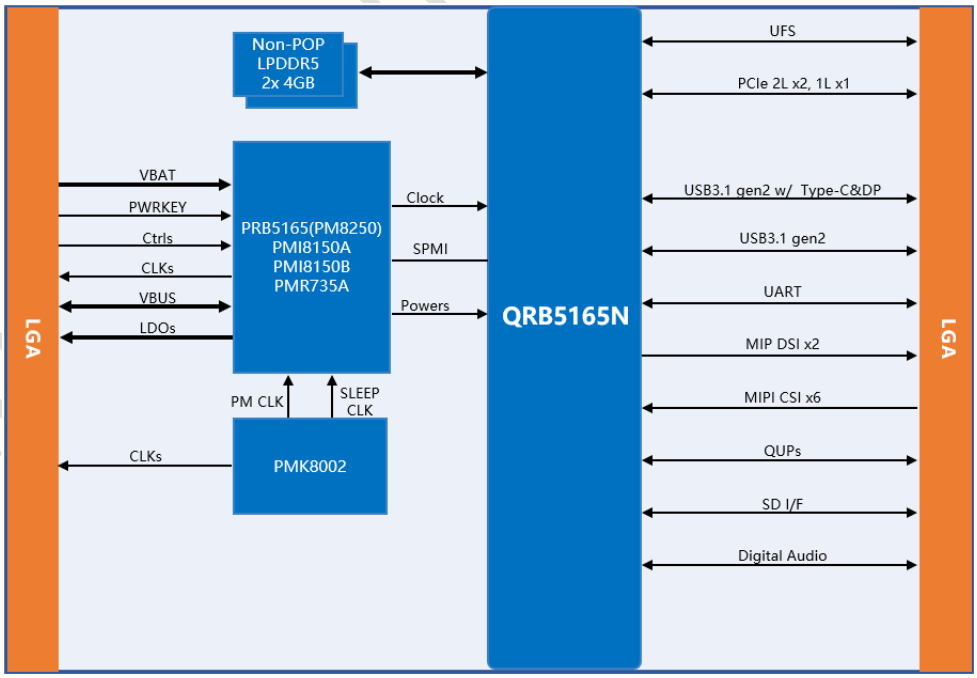


Figure 1-1.C5165N SOM Hardware Block Diagram

1.3. Major component location

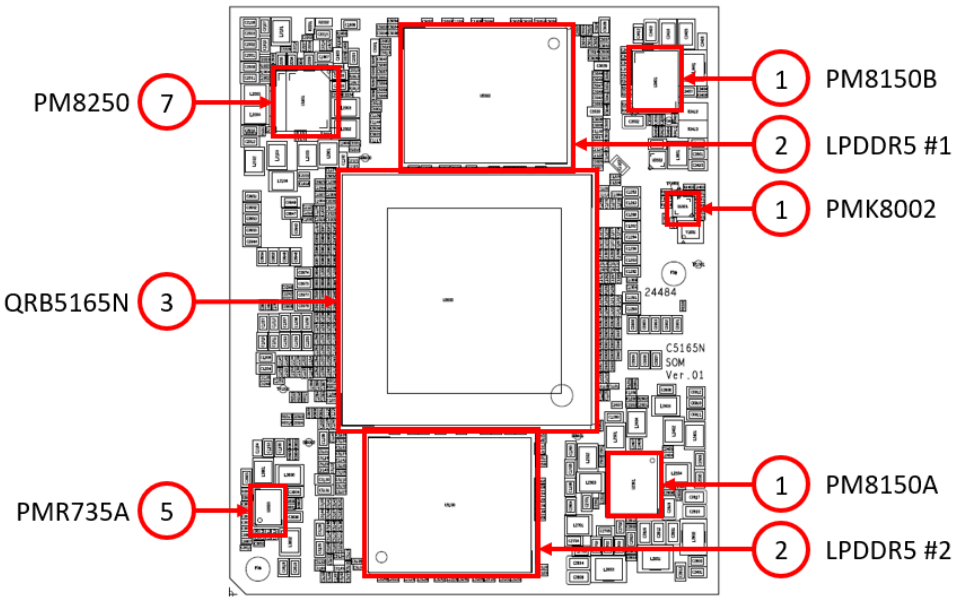


Figure 1-2. TurboX C5165N SOM Key Component Location

1.4. Mechanical size

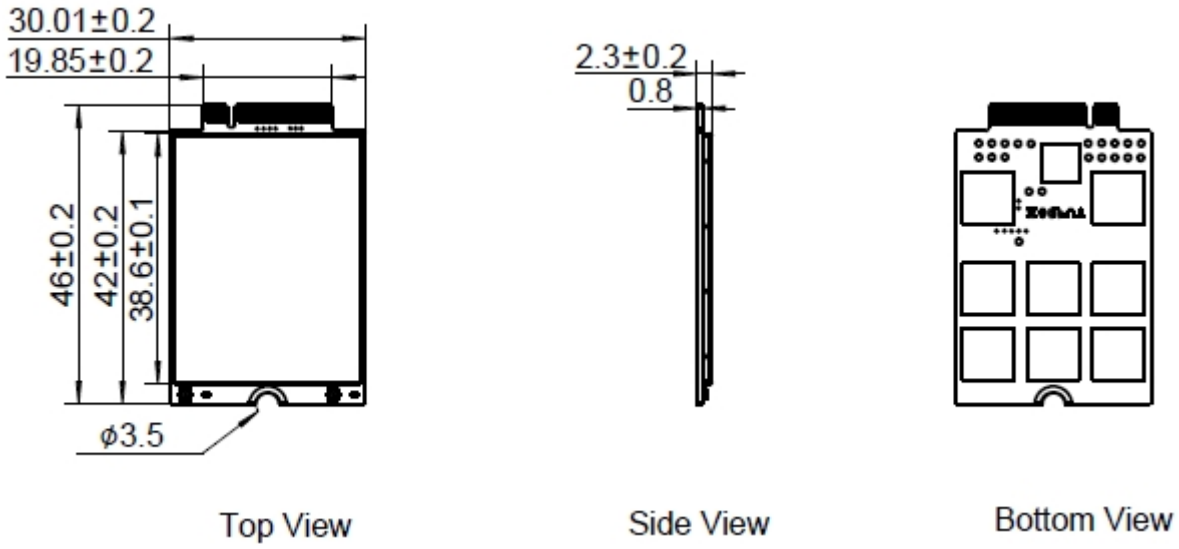


Figure 1-3. Mechanical Dimensions (SOM & Interposer Board)

1.5. Package dimensions

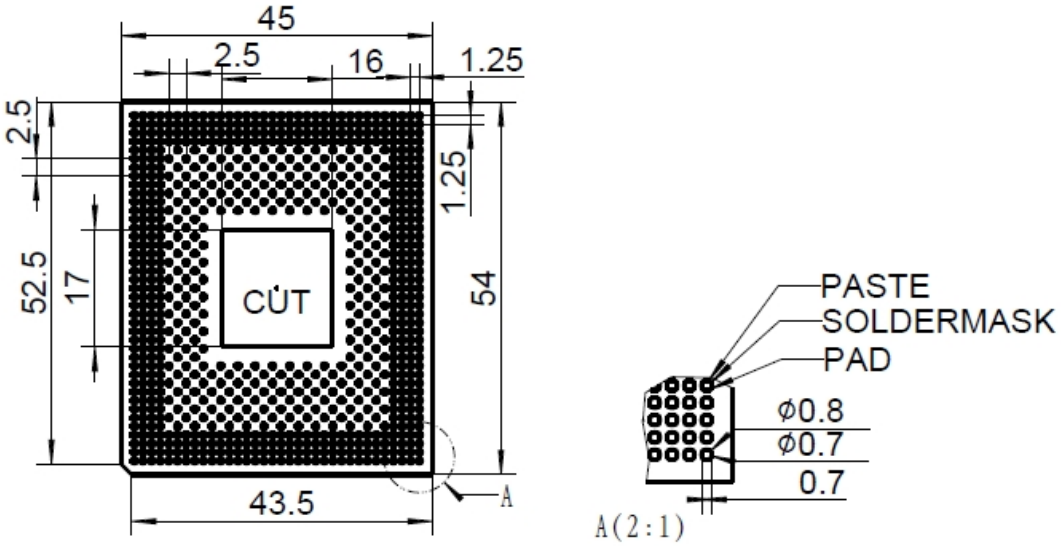


Figure 1-4. TurboX C5165N SOM Package Dimensions

1.6. Stencil design and aperture

To supply sufficient soldering paste and keep reliable soldering joints, add the thickness of stencil partly on the top surface. The stencil aperture for single sheet cannot be greater than 3.0mm×4.0mm and the exceeded part should be divided into smaller apertures with applicable shelves. A clearance of over 2.0mm should be kept between the outward end of the aperture and the component if there are components around the module.

➲ **NOTE**:

- For the convenience of heating and repairing, it is recommended that no components should be placed in the area at the backside of the module on PCB.
- In order to avoid reverse polarity of the module, it is recommended to use asymmetric pads at the bottom of the module to identify the module polarity during module placement.
- It is not recommended to add any silkscreen in the area where the module is mounted to avoid the height that may influence the solder paste printing and soldering quality.
- When there is a need to step-up the stencil, all 01005/0201, 0.4mm-pitch and 0.5mm-pitch components should be kept over 5.0mm away from the stepped-up area to avoid solder bridging that is caused by thicker solder paste.

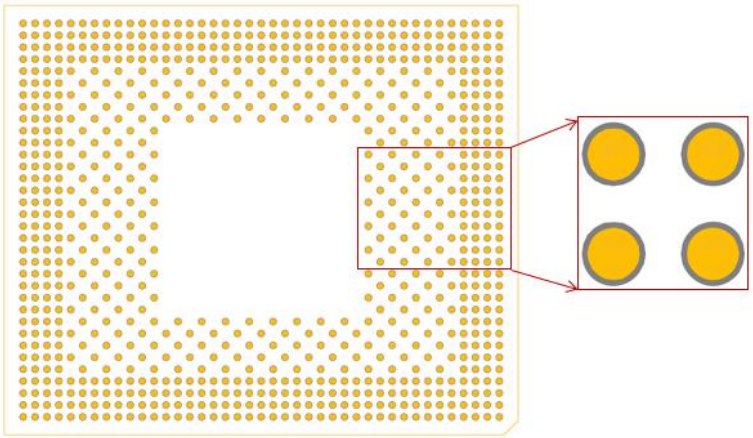


Figure 1-5.Stencil Aperture Diagram

Requirement description

- **Stencil thickness**
  Area of the module should be partly stepped-up to 0.15mm-0.18mm.

- **All pads stencil aperture**
  The aperture for each single pad should be centered with area reduced to 75%-85%. And the shape should be rectangle with round chamfers (as shown in Figure 1-5).

1.7. Module laser marking

Refer to Figure 1-2 for the module laser marking of TurboX C5165N.

Figure 1-6.Laser Marking of C5165N SOM

Table 1-3.Module laser marking description

1. Company name	5. Serial number
2. Product name	6. SOM brand
3. PCBA version	7. QR code
4. Product number	-

➲ **NOTE**:

- Figure 1-6 is for reference only and may vary with the specific module.
- The part number may be updated. Please confirm with the supplier about the accurate information.

1.8. SMT assembly guide

Refer to *TurboX Common SMT Assembly Guidelines.*

For more information, please contact us at service@thundercomm.com.

Chapter 2. Interface Specifications

This chapter introduces definitions of all the interfaces to facilitate design and verification on Thundercomm TurboX C5165N SOM.

2.1. Interface parameter definition

Table 2-1. Interfaces parameter definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DI	Digital input (CMOS)
DSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DO	Digital output (CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, it is 1.8V.
P2	SDC Power group 2, it is 1.8V or 2.95V.

2.2. Interface detailed description

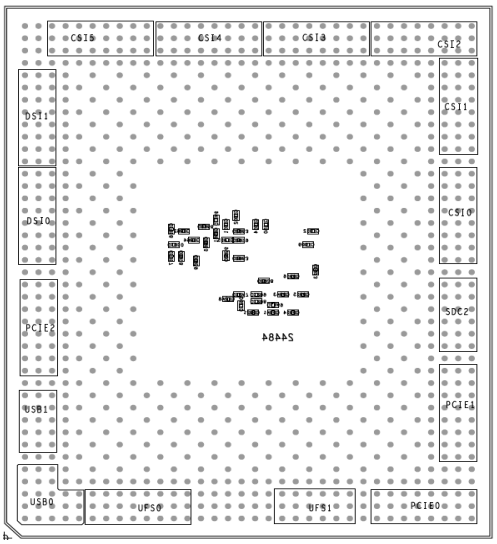


Figure 2-1. Pin Location ~~T~~top View)

2.2.1. Power supply interface

Table 2-2 describes all interfaces of SOM power supply. For the detailed parameter request, refer to Chapter 3. Electrical Characteristics.

Table 2-2. Power supply definition

Pin name	Pin	Type	Expected use (per IC spec)
VBATT	A485,A493,A501,A509,B702, B727,B754,B779	PI PO	Power supply input for SOM or output power for charging
USB0_VBUS	A162,A163,A164,A196,A197, B829,B854,B856	PI PO	Charger input power sources or output during USB-OTG operation.
VCOIN	A139	PI PO	Coin-cell charge and supply
VREG_BOB	A93,A94,A127,A128,B22	PO	Regulated BOB output
VREG_L2A_3P07	A190	PO	USB
VREG_L6A_1P2	A143,A144,B836	PO	UFS VCCQ, **for UFS only**
VREG_L7A_1P7	B707	PO	QCA VDDRFA backup
VREG_L12A_1P8	A146	PO	BBCLK, USB, UFS, QFPROM, **for internal use only**
VREG_L14A_1P8	B811	PO	OLED_VDDIO
VREG_L15A_1P8	A145	PO	QCA6436 VCC_1P8
VREG_L16A_3P3	A173	PO	EXT_BT_xPA 3P3
VREG_L17A_2P96	A140,A174	PO	UFS 2L VCC
VREG_S4A_1P8	A508,A516,A524	PO	Generic 1.8V power
VREG_S5A_1P9	A492,B703	PO	HV subregulated LDO
VREG_S6A_0P9	A239,A240	PO	LV subregulated LDO
VREG_L1C_1P8	B180	PO	LVS for camera
VREG_L2C_1P3	A285	PO	WCSS ADC – WCN RF
VREG_L3C_0P8	A293	PO	PHY: DSI – CSI
VREG_L4C_1P8	B103	PO	NFC – UICC1
VREG_L5C_1P8	B232	PO	NFC – UICC2
VREG_L7C_2P8	B74	PO	Sensors
VREG_L8C_1P8	B155	PO	LVS for sensors

Pin name	Pin	Type	Expected use (per IC spec)
VREG_L9C_2P9	A95,A129	PO	SD/MMC card or UFS card
VREG_L10C_3P0	A96	PO	WCN 3.3 V channel 1
VREG_L11C_3P3	B47	PO	WCN 3.3 V channel 0
VREG_S8C_1P3	A301,A309	PO	MV subregulated LDOs
VPH_PWR	A102,A135,A136,A171,A172, A205,A206	PI PO	Primary system supply node, SCHG regulated node
USB_IN_MID	A165,A166,A167,A168,A200, A201,A533,B858	PI	Mid point of the charger; input for charger buck; joint point for DC and wireless charging
VIO_OUT_PM_1P8	B234	PI	Connects to VREG_S4A; powers the internal dVdd domain, for PMIC only
PMK_DVDD_BYP	A531	PO	Internal dVdd regulator (1.5 V); with a 1 µF capacitor, for PMIC only
IUSB_OUT	A157	AO	Buffered voltage signal proportional to USB input current; Output to the charge pump. Regulates the input current limit with the charge pump.
PMR_VREG_L1	A109, A110	PO	L1 LDO regulated output of PMR735A
PMR_VREG_L2	A106, A276	PO	L2 LDO regulated output of PMR735A
PMR_VREG_L3	A107, A108	PO	L3 LDO regulated output of PMR735A
PMR_VREG_L4	B2	PO	L4 LDO regulated output of PMR735A
PMR_VREG_L5	A291, A291	PO	L5 LDO regulated output of PMR735A
PMR_VREG_L6	A300, B79	PO	L6 LDO regulated output of PMR735A
PMR_VREG_L7	A284, B27	PO	L7 LDO regulated output of PMR735A
PMR_VREG_S3G_2P2	A4,A5,A38,A39,A73	PO	L1 LDO regulated output of PMR735A

Pin name	Pin	Type	Expected use (per IC spec)
GND	A3,A6,A9,A12,A14,A15,A18,A19,A20,A23,A26,A32,A37,A42,A45,A47,A48,A54,A55,A57,A58,A59,A61,A62,A64,A65,A68,A69,A71,A72,A74,A75,A76,A77,A78,A79,A80,A81,A83,A84,A89,A90,A91,A92,A98,A100,A101,A105,A111,A115,A123,A126,A137,A147,A148,A149,A150,A151,A152,A153,A154,AA155,A156,A161,A169,A175,A176,A177,A178,A179,A180,A181,A182,A183,A184,A185,A186,A187,A188,A189,A191,A192,A194,A195,A198,A199,A202,A203,A204,A207,A208,A211,A214,A215,A216,A219,A222,A223,A224,A227,A230,A231,A234,A235,A238,A243,A246,A251,A254,A259,A262,A267,A270,A275,A280,A281,A283,A290,A295,A299,A302,A304,A305,A310,A314,A315,A316,A319,A323,A324,A326,A328,A329,A330,A331,A332,A333,A334,A338,A340,A341,A342,A343,A346,A348,A351,A352,A353,A356,A358,A359,A360,A363,A364,A366,A370,A371,A372,A374,A377,A379,A380,A382,A383,A387,A390,A391,A394,A398,A399,A401,A402,A406,A407,A408,A410,A414,A415,A418,A422,A425,A427,A429,A430,A432,A435,A437,A438,A439,A442,A443,A444,A446,A449,A454,A456,A463,A466,A474,A476,A477,A480,A482,A483,A486,A487,A489,A491,A494,A499,A500,A502,A504,A506,A507,A510,A511,A513,A515,A517,A518,A523,A525,A526,A528,A530,A532,A534,A535,B20,B29,B31,B35,B56,B70,B81,B87,B95,B106,B108,B131,B133,B139,B149,B158,B178,B183,B185,B191,B205,B207,B210,B212,B235,B237,B262,B264,B287,B289,B291,B314,B316,B339,B341,B343,B366,B420,B438,B517,B542,B544,B546,B569,B571,B594,B596,B599,B601,B603,B621,B626,B628,B646,B665,B667,B669,B671,B678,B680,B692,B694,B696,B705,B717,B719,B730,B732,B734,B736,B744,B746,B757,B759,B763,B769,B771,B790,B796,B804,B806,B815,B817,B819,B821,B823,B831,B844,B846,B848	GND	GND
Floating	A484,A138		

2.2.2. Display interface

The SOM supports 2x 4-lane MIPI DSI interfaces.

Table 2-3. Display interfaces definition

Pin name	Pin	Type	Description	Notes
DSI0_A0_LN0_P	A465	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – plus MIPI DSI 0 (CPHY), trio lane 0 – A	
DSI0_B0_LN0_M	A457	AI, AO	MIPI DSI 0 (DPHY), differential lane 0 – minus MIPI DSI 0 (CPHY), trio lane 0 – B	
DSI0_C0_LN1_P	A458	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – plus MIPI DSI 0 (CPHY), trio lane 0 – C	
DSI0_A1_LN1_M	A450	AI, AO	MIPI DSI 0 (DPHY), differential lane 1 – minus MIPI DSI 0 (CPHY), trio lane 1 – A	
DSI0_A2_LN2_P	A426	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – plus MIPI DSI 0 (CPHY), trio lane 2 – A	
DSI0_B2_LN2_M	A434	AI, AO	MIPI DSI 0 (DPHY), differential lane 2 – minus MIPI DSI 0 (CPHY), trio lane 2 – B	
DSI0_C2_LN3_P	A409	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – plus MIPI DSI 0 (CPHY), trio lane 2 – C	
DSI0_NC_LN3_M	A417	AI, AO	MIPI DSI 0 (DPHY), differential lane 3 – minus MIPI DSI 0 (CPHY), no connect	
DSI0_B1_CLK_P	A441	AI, AO	MIPI DSI 0 (DPHY), differential clock – plus MIPI DSI 0 (CPHY), trio lane 1 – B	
DSI0_C1_CLK_M	A433	AI, AO	MIPI DSI 0 (DPHY), differential clock – minus MIPI DSI 0 (CPHY), trio lane 1 – C	
DSI1_A0_LN0_P	A529	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – plus MIPI DSI 1 (CPHY), trio lane 0 – A	
DSI1_B0_LN0_M	A521	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – minus MIPI DSI 1 (CPHY), trio lane 0 – B	
DSI1_C0_LN1_P	A522	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – plus MIPI DSI 1 (CPHY), trio lane 0 – C	
DSI1_A1_LN1_M	A514	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – minus MIPI DSI 1 (CPHY), trio lane 1 – A	
DSI1_A2_LN2_P	A490	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – plus MIPI DSI 1 (CPHY), trio lane 2 – A	
DSI1_B2_LN2_M	A498	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – minus MIPI DSI 1 (CPHY), trio lane 2 – B	
DSI1_B1_CLK_P	A505	AI, AO	MIPI DSI 1 (DPHY), differential clock – plus MIPI DSI 1 (CPHY), trio lane 1 – B	
DSI1_C1_CLK_M	A497	AI, AO	MIPI DSI 1 (DPHY), differential clock – minus MIPI DSI 1 (CPHY), trio lane 1 – C	
DSI1_C2_LN3_P	A473	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – plus MIPI DSI 1 (CPHY), trio lane 2 – C	
DSI1_NC_LN3_M	A481	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – minus MIPI DSI 1 (CPHY), no connect	

2.2.3. Camera interfaces

The SOM supports 6x 4-lane D-PHY or 3-trio C-PHY camera interfaces.

Table 2-4. Camera interface definition

Pin name	Pin	Type	Decription	Notes
SM_I2C_CCI0_SCL	B45	IO	GPIO 102 Dedicated camera control interface I2C 0 clock	1.8V Pull up needed on Carrier board
SM_I2C_CCI0_SDA	A125	IO	GPIO 101 Dedicated camera control interface I2C 0 serial data	
SM_I2C_CCI1_SCL	B18	IO	GPIO 104 Dedicated camera control interface I2C 1 clock	
SM_I2C_CCI1_SDA	A124	IO	GPIO 103 Dedicated camera control interface I2C 1 serial data	
SM_I2C_CCI2_SCL	B174	IO	GPIO 106 Dedicated camera control interface I2C 2 clock	
SM_I2C_CCI2_SDA	B43	IO	GPIO 105 Dedicated camera control interface I2C 2 serial data	
SM_I2C_CCI3_SCL	A88	IO	GPIO 108 Dedicated camera control interface I2C 3 clock	
SM_I2C_CCI3_SDA	B122	IO	GPIO 107 Dedicated camera control interface I2C 3 serial data	
SM_CAM_MCLK0	A421	IO	GPIO 94 Camera master clock 0	
SM_CAM_MCLK1	A413	IO	GPIO 95 Camera master clock 1	
SM_CAM_MCLK2	B494	IO	GPIO 96 Camera master clock 2	
SM_CAM_MCLK3	A405	IO	GPIO 97 Camera master clock 3	
SM_CAM_MCLK4	B442	IO	GPIO 98 Camera master clock 4	
SM_CAM_MCLK5	A397	IO	GPIO 99 Camera master clock 5	
SM_CAM_MCLK6	A389	IO	GPIO 100 Camera master clock 6	
CSI0_NC_CLK_P	A416	AI, AO	MIPI CSI 0 (DPHY), differential clock – plus MIPI CSI 0 (CPHY), no connect	MIPI signals of Camera0
CSI0_A0_CLK_M	A424	AI, AO	MIPI CSI 0 (DPHY), differential clock – minus MIPI CSI 0 (CPHY), trio lane 0 – A	
CSI0_B0_LN0_P	A423	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – plus MIPI CSI 0 (CPHY), trio lane 0 – B	
CSI0_C0_LN0_M	A431	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – minus MIPI CSI 0 (CPHY), trio lane 0 – C	
CSI0_A1_LN1_P	A440	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – plus MIPI CSI 0 (CPHY), trio lane 1 – A	
CSI0_B1_LN1_M	A448	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – minus MIPI CSI 0 (CPHY), trio lane 1 – B	
CSI0_C1_LN2_P	A447	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – plus MIPI CSI 0 (CPHY), trio lane 1 – C	
CSI0_A2_LN2_M	A455	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – minus MIPI CSI 0 (CPHY), trio lane 2 – A	
CSI0_B2_LN3_P	A464	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – plus MIPI CSI 0 (CPHY), trio lane 2 – B	

Pin name	Pin	Type	Decription	Notes
CSI0_C2_LN3_M	A472	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – minus MIPI CSI 0 (CPHY), trio lane 2 – C	
CSI1_NC_CLK_P	A488	AI, AO	MIPI CSI 1 (DPHY), differential clock – plus MIPI CSI 1 (CPHY), no connect	MIPI signals of Camera1
CSI1_A0_CLK_M	A496	AI, AO	MIPI CSI 1 (DPHY), differential clock – minus MIPI CSI 1 (CPHY), trio lane 0 – A	
CSI1_B0_LN0_P	A495	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – plus MIPI CSI 1 (CPHY), trio lane 0 – B	
CSI1_C0_LN0_M	A503	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – minus MIPI CSI 1 (CPHY), trio lane 0 – C	
CSI1_A1_LN1_P	A512	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – plus MIPI CSI 1 (CPHY), trio lane 1 – A	
CSI1_B1_LN1_M	A520	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – minus MIPI CSI 1 (CPHY), trio lane 1 – B	
CSI1_C1_LN2_P	A519	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – plus MIPI CSI 1 (CPHY), trio lane 1 – C	
CSI1_A2_LN2_M	A527	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – minus MIPI CSI 1 (CPHY), trio lane 2 – A	
CSI1_B2_LN3_P	A536	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – plus MIPI CSI 1 (CPHY), trio lane 2 – B	
CSI1_C2_LN3_M	A170	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – minus MIPI CSI 1 (CPHY), trio lane 2 – C	
CSI2_NC_CLK_P	A272	AI, AO	MIPI CSI 2 (DPHY), differential clock – plus MIPI CSI 2 (CPHY), no connect	MIPI signals of Camera2
CSI2_A0_CLK_M	A271	AI, AO	MIPI CSI 2 (DPHY), differential clock – minus MIPI CSI 2 (CPHY), trio lane 0 – A	
CSI2_B0_LN0_P	A237	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – plus MIPI CSI 2 (CPHY), trio lane 0 – B	
CSI2_C0_LN0_M	A236	AI, AO	MIPI CSI 2 (DPHY), differential lane 0 – minus MIPI CSI 2 (CPHY), trio lane 0 – C	
CSI2_A1_LN1_P	A269	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – plus MIPI CSI 2 (CPHY), trio lane 1 – A	
CSI2_B1_LN1_M	A268	AI, AO	MIPI CSI 2 (DPHY), differential lane 1 – minus MIPI CSI 2 (CPHY), trio lane 1 – B	
CSI2_C1_LN2_P	A233	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – plus MIPI CSI 2 (CPHY), trio lane 1 – C	
CSI2_A2_LN2_M	A232	AI, AO	MIPI CSI 2 (DPHY), differential lane 2 – minus MIPI CSI 2 (CPHY), trio lane 2 – A	
CSI2_B2_LN3_P	A266	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – plus MIPI CSI 2 (CPHY), trio lane 2 – B	
CSI2_C2_LN3_M	A265	AI, AO	MIPI CSI 2 (DPHY), differential lane 3 – minus MIPI CSI 2 (CPHY), trio lane 2 – C	
CSI3_NC_CLK_P	A264	AI, AO	MIPI CSI 3 (DPHY), differential clock – plus MIPI CSI 3 (CPHY), no connect	MIPI signals of Camera3
CSI3_A0_CLK_M	A263	AI, AO	MIPI CSI 3 (DPHY), differential clock – minus MIPI CSI 3 (CPHY), trio lane 0 – A	
CSI3_B0_LN0_P	A229	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – plus MIPI CSI 3 (CPHY), trio lane 0 – B	
CSI3_C0_LN0_M	A228	AI, AO	MIPI CSI 3 (DPHY), differential lane 0 – minus MIPI CSI 3 (CPHY), trio lane 0 – C	
CSI3_A1_LN1_P	A261	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – plus MIPI CSI 3 (CPHY), trio lane 1 – A	

Pin name	Pin	Type	Decription	Notes
CSI3_B1_LN1_M	A260	AI, AO	MIPI CSI 3 (DPHY), differential lane 1 – minus MIPI CSI 3 (CPHY), trio lane 1 – B	
CSI3_C1_LN2_P	A226	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – plus MIPI CSI 3 (CPHY), trio lane 1 – C	
CSI3_A2_LN2_M	A225	AI, AO	MIPI CSI 3 (DPHY), differential lane 2 – minus MIPI CSI 3 (CPHY), trio lane 2 – A	
CSI3_B2_LN3_P	A258	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – plus MIPI CSI 3 (CPHY), trio lane 2 – B	
CSI3_C2_LN3_M	A257	AI, AO	MIPI CSI 3 (DPHY), differential lane 3 – minus MIPI CSI 3 (CPHY), trio lane 2 – C	
CSI4_NC_CLK_P	A256	AI, AO	MIPI CSI 4 (DPHY), differential clock – plus MIPI CSI 4 (CPHY), no connect	MIPI signals of Camera4
CSI4_A0_CLK_M	A255	AI, AO	MIPI CSI 4 (DPHY), differential clock – minus MIPI CSI 4 (CPHY), trio lane 0 – A	
CSI4_B0_LN0_P	A221	AI, AO	MIPI CSI 4 (DPHY), differential lane 0 – plus MIPI CSI 4 (CPHY), trio lane 0 – B	
CSI4_C0_LN0_M	A220	AI, AO	MIPI CSI 4 (DPHY), differential lane 0 – minus MIPI CSI 4 (CPHY), trio lane 0 – C	
CSI4_A1_LN1_P	A253	AI, AO	MIPI CSI 4 (DPHY), differential lane 1 – plus MIPI CSI 4 (CPHY), trio lane 1 – A	
CSI4_B1_LN1_M	A252	AI, AO	MIPI CSI 4 (DPHY), differential lane 1 – minus MIPI CSI 4 (CPHY), trio lane 1 – B	
CSI4_C1_LN2_P	A218	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 – plus MIPI CSI 4 (CPHY), trio lane 1 – C	
CSI4_A2_LN2_M	A217	AI, AO	MIPI CSI 4 (DPHY), differential lane 2 – minus MIPI CSI 4 (CPHY), trio lane 2 – A	
CSI4_B2_LN3_P	A250	AI, AO	MIPI CSI 4 (DPHY), differential lane 3 – plus MIPI CSI 4 (CPHY), trio lane 2 – B	
CSI4_C2_LN3_M	A249	AI, AO	MIPI CSI 4 (DPHY), differential lane 3 – minus MIPI CSI 4 (CPHY), trio lane 2 – C	
CSI5_NC_CLK_P	A248	AI, AO	MIPI CSI 5 (DPHY), differential clock – plus MIPI CSI 5 (CPHY), no connect	MIPI signals of Camera5
CSI5_A0_CLK_M	A247	AI, AO	MIPI CSI 5 (DPHY), differential clock – minus MIPI CSI 5 (CPHY), trio lane 0 – A	
CSI5_B0_LN0_P	A213	AI, AO	MIPI CSI 5 (DPHY), differential lane 0 – plus MIPI CSI 5 (CPHY), trio lane 0 – B	
CSI5_C0_LN0_M	A212	AI, AO	MIPI CSI 5 (DPHY), differential lane 0 – minus MIPI CSI 5 (CPHY), trio lane 0 – C	
CSI5_A1_LN1_P	A245	AI, AO	MIPI CSI 5 (DPHY), differential lane 1 – plus MIPI CSI 5 (CPHY), trio lane 1 – A	
CSI5_B1_LN1_M	A244	AI, AO	MIPI CSI 5 (DPHY), differential lane 1 – minus MIPI CSI 5 (CPHY), trio lane 1 – B	
CSI5_C1_LN2_P	A210	AI, AO	MIPI CSI 5 (DPHY), differential lane 2 – plus MIPI CSI 5 (CPHY), trio lane 1 – C	
CSI5_A2_LN2_M	A209	AI, AO	MIPI CSI 5 (DPHY), differential lane 2 – minus MIPI CSI 5 (CPHY), trio lane 2 – A	
CSI5_B2_LN3_P	A242	AI, AO	MIPI CSI 5 (DPHY), differential lane 3 – plus MIPI CSI 5 (CPHY), trio lane 2 – B	
CSI5_C2_LN3_M	A241	AI, AO	MIPI CSI 5 (DPHY), differential lane 3 – minus MIPI CSI 5 (CPHY), trio lane 2 – C	

2.2.4. Audio interface

The SOM provides Soundwire, SLIMbus, DMIC and I2S interfaces for audio. Soundwire interface is special for external codec IC, which can build audio functions of the systeme. DMIC interface can be used to directly connect up to 6 PDM MICs.

Table 2-5. Audio interface definition

Pin name	Pin	Voltage	Type	Description	Notes
SM_DMIC01_CLK	B137	1.8	IO	GPIO 152 DMIC1 clock LPI_MI2S1_CLK	LPI_MI2S1
SM_DMIC01_DATA	B58	1.8	IO	GPIO 153 DMIC1 data LPI_MI2S1_WS	
SM_DMIC23_CLK	B189	1.8	IO	GPIO 154 DMIC2 clock LPI_MI2S1_DATA0	
SM_DMIC23_DATA	B110	1.8	IO	GPIO 155 DMIC2 data LPI_MI2S1_DATA1	
SM_DMIC45_CLK	B60	1.8	IO	GPIO 158 DMIC3 clock LPI_MI2S2_DATA0	LPI_MI2S2
SM_DMIC45_DATA	B85	1.8	IO	GPIO 159 DMIC3 data LPI_MI2S2_DATA1	
SM_SWR_WCD_RX_CLK	A112	1.8	IO	GPIO 149 SoundWire receive clock LPI_MI2S0_DATA1	LPI_MI2S0
SM_SWR_WCD_RX_DATA0	B33	1.8	IO	GPIO 150 SoundWire receive data 0 LPI_MI2S0_DATA2	
SM_SWR_WCD_RX_DATA1	B6	1.8	IO	GPIO 151 SoundWire receive data 1 LPI_MI2S0_DATA3	
SM_SWR_WCD_TX_CLK	A114	1.8	IO	GPIO 146 SoundWire transmit clock LPI_MI2S0_SCK	
SM_SWR_WCD_TX_DATA0	B8	1.8	IO	GPIO 147 SoundWire transmit data 0 LPI_MI2S0_WS	
SM_SWR_WCD_TX_DATA1	A113	1.8	IO	GPIO 148 SoundWire transmit data 1 LPI_MI2S0_DATA0	
SM_SWR_WSA_CLK	B112	1.8	IO	GPIO 156 SoundWire clock for WSA LPI_MI2S2_CLK	LPI_MI2S2
SM_SWR_WSA_DATA	B164	1.8	IO	GPIO 157 SoundWire data for WSA LPI_MI2S2_WS	
SM_SLIMBUS_HST_CLK	B91	1.8	IO	GPIO 142 Low-power audio SLIMbus clock MI2S1_SCK	MI2S1
SM_SLIMBUS_HST_DATA	B143	1.8	IO	GPIO 143 Low-power audio SLIMbus data 0 MI2S1_DATA0	
SM_GPIO_133	A86	1.8	IO	GPIO 133 MI2S2_SCK	MI2S2
SM_GPIO_134	A120	1.8	IO	GPIO 134 MI2S2_DATA0	

Pin name	Pin	Voltage	Type	Description	Notes
SM_GPIO_135	B14	1.8	IO	GPIO 135 MI2S2_WS	
SM_GPIO_136	B66	1.8	IO	GPIO 136 MI2S0_MCLK	MI2S0
SM_GPIO_137	B118	1.8	IO	GPIO 137 MI2S1_MCLK MI2S2_DATA1	MI2S1 or MI2S2
SM_GPIO_138	B170	1.8	IO	GPIO 138 MI2S0_SCK	MI2S0
SM_GPIO_139	A85	1.8	IO	GPIO 139 MI2S0_DATA0	
SM_GPIO_140	A119	1.8	IO	GPIO 140 MI2S0_DATA1	
SM_GPIO_141	B39	1.8	IO	GPIO 141 MI2S0_WS	
SM_GPIO_144	B195	1.8	IO	GPIO 144 LPASS_SLIMBUS_DATA1 MI2S1_DATA1	MI2S1
SM_GPIO_145	A51	1.8	IO	GPIOI 145 LPASS_SLIMBUS_DATA2 MI2S1_WS	

2.2.5. USB & DisplayPort interface

The SOM supports 2x USB 3.1 ports, support Type-C with DisplayPort v1.4 in one port.

Table 2-6. USB &DP interface definition

Pin name	Pin	Type	Description	Note
SM_USB0_HS_DM	A70	AI, AO	USB high-speed 0 data – minus	
SM_USB0_HS_DP	A104	AI, AO	USB high-speed 0 data – plus	
SM_USB0_SS_RX0_M	A36	AI	USB super-speed 0 receive 0 – minus	
SM_USB0_SS_RX0_P	A2	AI	USB super-speed 0 receive 0 – plus	
SM_USB0_SS_TX0_M	A35	AO	USB super-speed 0 transmit 0 – minus	
SM_USB0_SS_TX0_P	A1	AO	USB super-speed 0 transmit 0 – plus	
SM_USB0_SS_RX1_M	A274	AI	USB super-speed 0 receive 1 – minus	
SM_USB0_SS_RX1_P	A282	AI	USB super-speed 0 receive 1 – plus	
SM_USB0_SS_TX1_M	A103	AO	USB super-speed 0 transmit 1 – minus	
SM_USB0_SS_TX1_P	A273	AO	USB super-speed 0 transmit 1 – plus	
SM_USB1_HS_D_M	A297	AI, AO	USB high-speed 1 data – minus	
SM_USB1_HS_D_P	A289	AI, AO	USB high-speed 1 data – plus	
SM_USB1_ID	A322	IO	GPIO 91 USB ID	
SM_USB1_SS_RX_M	A306	AI	USB super-speed 1 receive – minus	
SM_USB1_SS_RX_P	A298	AI	USB super-speed 1 receive – plus	
SM_USB1_SS_TX_M	A321	AO	USB super-speed 1 transmit – minus	
SM_USB1_SS_TX_P	A313	AO	USB super-speed 1 transmit – plus	
USB0_CC1	B852	AI	OTG mode enable or CC1 pin for USB Type-C connector (user programmable); 22 V protected	
USB0_CC2	B850	AI	CC2 pin for USB Type-C connector; 22 V protected	

Pin name	Pin	Type	Description	Note
PM_USB_SBU1	B825	DI	SBU1 pin from the USB Type-C connector; 22 V protected	
PM_USB_SBU2	A160	DI	SBU2 pin from the USB Type-C connector; 22 V protected	
SM_USB0_CC_DIR	A420	IO	GPIO 65 USB PHY Port select	
EDP_AUX_M	B472	AI,AO	DisplayPort auxiliary channel – minus	
EDP_AUX_P	B497	AI,AO	DisplayPort auxiliary channel – plus	

2.2.6. PCIe interface

The SOM support Peripheral Component Interconnect Express (PCIe) interfaces.

Table 2-7. PCIe interface definition

Pin name	Pin	Type	Description	Notes
SM_PCIE0_CLK_REQ_N	A28	IO	GPIO 80 PCIE0 CLK REQ N	
SM_PCIE0_RST_N	A29	IO	GPIO 79 PCIE0 RESET	
SM_PCIE0_WAKE_N	A27	IO	GPIO 81	
PCIE0_REFCLK_M	A66	AO	PCIe 0 Gen 3 reference clock – minus	
PCIE0_REFCLK_P	A67	AO	PCIe 0 Gen 3 reference clock – plus	
PCIE0_RX0_M	A34	AI	PCIe 0 Gen 3 receive – minus	
PCIE0_RX0_P	A33	AI	PCIe 0 Gen 3 receive – plus	
PCIE0_TX0_M	A30	AO	PCIe 0 Gen 3 transmit – minus	
PCIE0_TX0_P	A31	AO	PCIe 0 Gen 3 transmit – plus	
SM_PCIE1_CLK_REQ_N	A287	IO	GPIO 83 PCIE1 CLK REQ N	
SM_PCIE1_RST_N	A294	IO	GPIO 82 PCIE1 RESET	
SM_PCIE1_WAKE_N	A286	IO	GPIO 84	
PCIE1_REFCLK_M	A336	AO	PCIe 1 Gen 3 reference clock – minus	
PCIE1_REFCLK_P	A344	AO	PCIe 1 Gen 3 reference clock – plus	
PCIE1_RX0_M	A311	AI	PCIe 1 Gen 3 receive 0 – minus	
PCIE1_RX0_P	A303	AI	PCIe 1 Gen 3 receive 0 – plus	
PCIE1_TX0_M	A320	AO	PCIe 1 Gen 3 transmit 0 – minus	
PCIE1_TX0_P	A312	AO	PCIe 1 Gen 3 transmit 0 – plus	
PCIE1_RX1_M	A288	AI	PCIe 1 Gen 3 receive 1 – minus	
PCIE1_RX1_P	A296	AI	PCIe 1 Gen 3 receive 1 – plus	
PCIE1_TX1_M	A335	AO	PCIe 1 Gen 3 transmit 1 – minus	
PCIE1_TX1_P	A327	AO	PCIe 1 Gen 3 transmit 1 – plus	
SM_PCIE2_CLK_REQ_N	A347	IO	GPIO 86 PCIE2 CLK REQ N	
SM_PCIE2_RST_N	A339	IO	GPIO 85 PCIE2 RESET	
SM_PCIE2_WAKE_N	A355	IO	GPIO 87	

Pin name	Pin	Type	Description	Notes
PCIE2_REFCLK_M	A361	AO	PCIe 2 Gen 3 reference clock – minus	
PCIE2_REFCLK_P	A369	AO	PCIe 2 Gen 3 reference clock – plus	
PCIE2_RX0_M	A337	AI	PCIe 2 Gen 3 receive 0 – minus	
PCIE2_RX0_P	A345	AI	PCIe 2 Gen 3 receive 0 – plus	
PCIE2_TX0_M	A385	AO	PCIe 2 Gen 3 transmit 0 – minus	
PCIE2_TX0_P	A393	AO	PCIe 2 Gen 3 transmit 0 – plus	
PCIE2_RX1_M	A362	AI	PCIe 2 Gen 3 receive 1 – minus	
PCIE2_RX1_P	A354	AI	PCIe 2 Gen 3 receive 1 – plus	
PCIE2_TX1_M	A378	AO	PCIe 2 Gen 3 transmit 1 – minus	
PCIE2_TX1_P	A386	AO	PCIe 2 Gen 3 transmit 1 – plus	

2.2.7. SSC interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

Table 2-8. SSC interface definition

Pin name	Pin	Voltage	Type	Function Description	Notes
SM_SNS_I3C0_SDA	A118	1.8	IO	GPIO 160 SSC I/O 0	
SM_SNS_I3C0_SCL	B193	1.8	IO	GPIO 161 SSC I/O 1	
SM_OIS_I3C1_SDA	B141	1.8	IO	GPIO 162 SSC I/O 2	
SM_OIS_I3C1_SCL	B37	1.8	IO	GPIO 163 SSC I/O 3	
SM_GPIO_164	B10	1.8	IO	Configurable I/O SSC I/O 4	
SM_GPIO_165	A82	1.8	IO	Configurable I/O SSC I/O 5	
SM_GPIO_166	B62	1.8	IO	Configurable I/O SSC I/O 6	
SM_GPIO_167	A116	1.8	IO	Configurable I/O SSC I/O 7	
SM_OIS2_I2C3_SDA	B89	1.8	IO	GPIO 168 SSC I/O 8	
SM_OIS2_I2C3_SCL	A117	1.8	IO	GPIO 169 SSC I/O 9	
SM_SNS_I2C4_SDA	B166	1.8	IO	GPIO 170 SSC I/O 10	
SM_SNS_I2C4_SCL	B114	1.8	IO	GPIO 171 SSC I/O 11	
SM_GPIO_172	B168	1.8	IO	Configurable I/O SSC I/O 12	
SM_GPIO_173	B116	1.8	IO	Configurable I/O SSC I/O 13	
SM_GPIO_174	B64	1.8	IO	Configurable I/O SSC I/O 14	
SM_GPIO_175	B12	1.8	IO	Configurable I/O SSC I/O 15	
SM_UART_HST_BLE_TX	A17	1.8	IO	GPIO 176 SSC I/O 16	

Pin name	Pin	Voltage	Type	Function Description	Notes
SM_UART_HST_BLE_RX	A16	1.8	IO	GPIO 177 SSC I/O 17	
SM_UART_HST_WL_TX	A50	1.8	IO	GPIO 178 SSC I/O 18	
SM_UART_HST_WL_RX	A49	1.8	IO	GPIO 179 SSC I/O 19	

2.2.8. SDIO interface

The SOM support dual 4-laneSDIO, SDC2 for SD-card and SDC4.

The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 MHz.
- The signals routing should be 50ohm ±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

Table 2-9. SDIO interface definition

PIN Name	PIN	Voltage	Type	Function Description	Notes
SM_SDC2_CLK	A375	1.8 or 2.95	DO	Secure digital controller 2 clock	
SM_SDC2_CMD	A400	1.8 or 2.95	IO	Secure digital controller 2 command	
SM_SDC2_DATA_0	A368	1.8 or 2.95	IO	Secure digital controller 2 data bit 0	
SM_SDC2_DATA_1	A376	1.8 or 2.95	IO	Secure digital controller 2 data bit 1	
SM_SDC2_DATA_2	A384	1.8 or 2.95	IO	Secure digital controller 2 data bit 2	
SM_SDC2_DATA_3	A392	1.8 or 2.95	IO	Secure digital controller 2 data bit 3	
SM_SD_CARD_DET_N	A367	1.8	DI	GPIO 77 SD Card detection	
SM_SDC4_CLK	A468	1.8	IO	GPIO 73 Secure digital controller 4 clock Quad-SPI clock	
SM_SDC4_CMD	A460	1.8	IO	GPIO 71 Secure digital controller 4 command Quad-SPI data bit 1	
SM_SDC4_DATA_0	A452	1.8	IO	GPIO 76 Secure digital controller 4 clock data bit 0	
SM_SDC4_DATA_1	A451	1.8	IO	GPIO 75 Secure digital controller 4 clock data bit 1 Quad-SPI chip select 1	
SM_SDC4_DATA_2	A467	1.8	IO	GPIO 74 Secure digital controller 4 clock data bit 2 Quad-SPI data bit 3	
SM_SDC4_DATA_3	A459	1.8	IO	GPIO 72 Secure digital controller 4 clock data bit 3 Quad-SPI data bit 2	

2.2.9. GPIO &QUP interface

These GPIOs are available as QUP (Qualcomm universal peripheral) interface ports that can be configured for UART, SPI, I2C or I3C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus needs to be supplemented by a 2.2 kΩ pull-up resistor.

Table 2-10. QUP Ports

Generic I/O	UART	I2C	SPI	I3C
QUP_L0	CTS	SDA	MISO	SDA
QUP_L1	RFR	SCL	MOSI	SCL
QUP_L2	Tx	-	SCLK	-
QUP_L3	Rx	-	CS_0	-
QUP_L4	-	-	CS_1	-
QUP_L5	-	-	CS_2	-
QUP_L6	-	-	CS_3	-

Table 2-11. QUP interface definition

Pin name	Pin	Voltage	Wakeup	QUP	Notes
SM_GPIO_00	A428	1.8	IO	QUP_L0(19)	
SM_GPIO_01	B447	1.8	IO	QUP_L1(19)	
SM_GPIO_02	B524	1.8	IO	QUP_L2(19)	
SM_GPIO_03	B495	1.8	IO	QUP_L3(19)	
SM_GPIO_04	B390	1.8	IO	QUP_L0(1)	
SM_GPIO_05	A373	1.8	IO	QUP_L1(1)	
SM_GPIO_06	B338	1.8	IO	QUP_L2(1)	
SM_GPIO_07	B388	1.8	IO	QUP_L3(1)	
SM_GPIO_08	B386	1.8	IO	QUP_L0(4)	
SM_GPIO_09	A350	1.8	IO	QUP_L1(4)	
SM_GPIO_10	B309	1.8	IO	QUP_L2(4)	
SM_GPIO_11	B259	1.8	IO	QUP_L3(4)	
SM_GPIO_12	B334	1.8	IO	QUP_L0(5)	
SM_GPIO_13	B257	1.8	IO	QUP_L1(5)	
SM_GPIO_14	A349	1.8	IO	QUP_L2(5)	
SM_GPIO_15	B284	1.8	IO	QUP_L3(5)	
SM_GPIO_22	B176	1.8	IO	QUP_L2(7)	
SM_GPIO_23	B97	1.8	IO	QUP_L3(7)	
SM_GPIO_24	B742	1.8	IO	QUP_L0(8)	
SM_GPIO_25	B160	1.8	IO	QUP_L1(8)	
SM_GPIO_26	B368	1.8	IO	QUP_L2(8)	
SM_FAST_BOOT_0	B767	1.8	IO	QUP_L3(8), GPIO 27 BOOT_CONFIG(1)	
SM_GPIO_28	B467	1.8	IO	QUP_L0(0)	
SM_GPIO_29	B465	1.8	IO	QUP_L1(0)	
SM_GPIO_30	B415	1.8	IO	QUP_L2(0)	
SM_GPIO_31	A381	1.8	IO	QUP_L3(0)	
SM_GPIO_32	A388	1.8	IO	QUP_L0(12)	
SM_GPIO_33	B391	1.8	IO	QUP_L1(12)	
SM_GPIO_36	B393	1.8	IO	QUP_L0(13)	
SM_GPIO_37	A396	1.8	IO	QUP_L1(13)	
SM_GPIO_38	B395	1.8	IO	QUP_L2(13)	
SM_GPIO_39	A403	1.8	IO	QUP_L3(13)	
SM_GPIO_40	B653	1.8	IO	QUP_L0(14)	

Pin name	Pin	Voltage	Wakeup	QUP	Notes
SM_GPIO_41	A475	1.8	IO	QUP_L1(14)	
SM_GPIO_42	B657	1.8	IO	QUP_L2(14)	
SM_GPIO_43	B655	1.8	IO	QUP_L3(14)	
SM_I2C_APPS_SDA	A419	1.8	IO	QUP_L0(15), GPIO 44	
SM_I2C_APPS_SCL	A411	1.8	IO	QUP_L1(15), GPIO 45	
SM_GPIO_46	B470	1.8	IO	QUP_L2(15)	
SM_FAST_BOOT_1	A412	1.8	IO	QUP_L3(15), QUP_L5(14) GPIO 47 Fast boot bit 1	
SM_GPIO_48	B443	1.8	IO	QUP_L0(16)	
SM_GPIO_49	B418	1.8	IO	QUP_L1(16)	
SM_GPIO_50	A404	1.8	IO	QUP_L2(16)	
SM_GPIO_51	A395	1.8	IO	QUP_L3(16)	
SM_GPIO_52	B499	1.8	IO	QUP_L0(17)	
SM_GPIO_53	A436	1.8	IO	QUP_L1(17)	
SM_GPIO_54	B522	1.8	IO	QUP_L2(17)	
SM_GPIO_55	B549	1.8	IO	QUP_L3(17)	
SM_GPIO_56	B547	1.8	IO	QUP_L0(18)	
SM_GPIO_57	B574	1.8	IO	QUP_L1(18)	
SM_GPIO_58	B576	1.8	IO	QUP_L2(18)	
SM_GPIO_59	B684	1.8	IO	QUP_L3(18)	
SM_GPIO_60	B83	1.8	IO	QUP_L0(11)	
SM_GPIO_61	B135	1.8	IO	QUP_L1(11)	
SM_GPIO_62	B187	1.8	IO	QUP_L2(11)	
SM_GPIO_63	B239	1.8	IO	QUP_L3(11)	
SM_GPIO_64	B445	1.8	IO	QUP_L6(14)	
SM_GPIO_92	B147	1.8	IO	QUP_L6(4)	
SM_GPIO_93	B199	1.8	IO	QUP_L6(2)	
SM_GPIO_115	B363	1.8	IO	QUP_L0(2)	
SM_GPIO_116	B413	1.8	IO	QUP_L1(2)	
SM_GPIO_117	A365	1.8	IO	QUP_L2(2)	
SM_GPIO_118	A357	1.8	IO	QUP_L3(2)	
SM_GPIO_119	B336	1.8	IO	QUP_L0(3)	
SM_GPIO_120	B286	1.8	IO	QUP_L1(3)	
SM_HALL_INT_N	B311	1.8	IO	QUP_L2(3), GPIO 121	
SM_ALSP_INT_N	B361	1.8	IO	QUP_L3(3), GPIO 122	
SM_IMU1_INT	A52	1.8	IO	QUP_L4(4), GPIO 123	
SM_GPIO_125	B663	1.8	IO	QUP_L0(9)	
SM_GPIO_126	B792	1.8	IO	QUP_L1(9)	
SM_GPIO_127	B715	1.8	IO	QUP_L2(9)	
SM_WDOG_DISABLE	B765	1.8	IO	QUP_L3(9), GPIO 128 Boot configuration bit 0	Boot function only active during boot
SM_PRESS_INT	B740	1.8	IO	QUP_L0(10), GPIO 129	
SM_GPIO_130	B688	1.8	IO	QUP_L1(10)	
SM_GPIO_131	B711	1.8	IO	QUP_L2(10)	
SM_FORCED_USB_BOOT	B659	1.8	IO	QUP_L3(10)	Boot function only active during boot

2.2.10. Power on interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, and enable the correct source. It takes more than 1s to press the power on button for power on event. And it is suggested for 3s powering on system. Power on/off key signal can be connected to ground through PM_KYPD_PWR_N; the other power on method is: when using CBL_PWR_N pin connect to ground, insert battery or power supply, SOM will power on automatically.

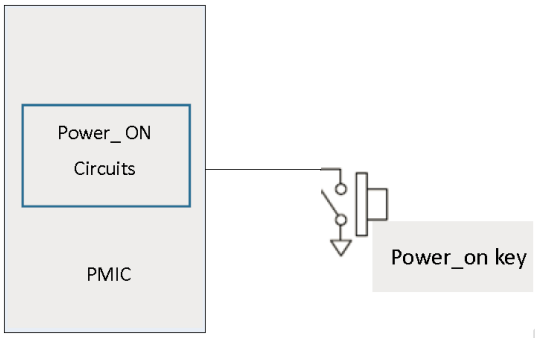


Figure 2-1.Power on Signal

Table 2-12. Power on interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PM_KYPD_PWR_N	A158	-	DI	Power-on key ground switch (200 kΩ internal PU to 1.1 V)	
CBL_PWR_N	B842		DI	Cable power-on ground switch (200 kohm internal PU to 1.8 V)	

2.2.11. Reset interface

Extended press of volume key will initiate a shutdown or reset (software selectable)

- Stage 1 reset – software-configurable bark

  PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

  If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

  The user can generate a mandatory reset by a long press of KYPD_VOLDN_N, or PM_KYPD_PWR_N, or KYPD_VOLDN_N+PM_KYPD_PWR_N in combination.

The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers

Table 2-13. Reset interface definition

Pin name	Pin	Voltage	Type	Description	Notes
KYPD_VOLDN_N	B813	pulled up internally to 1.8V	DI	Volume down/Reset key signal, Low active	

2.2.12. Keys interface

Table 2-14. Keys interface definition

Pin name	Pin	Voltage	Type	Description	Notes
KYPD_VOLUP_N	B761	-	DI	Keypad volume up button	
KYPD_VOLDN_N	B813	40 kΩ internal PU to 1.8 V	DI	Reset Keypad volume down button	

2.2.13. Debug UART interface

Table 2-15. Debug UART interface definition

Pin name	Pin	Voltage	Type	Function Description	Notes
SM_UART_DEBUG_RX	B661	1.8	IO	GPIO 35 QUP 12, lane 3: SPI_CS_0/UART_RX	
SM_UART_DEBUG_TX	B686	1.8	IO	GPIO 34 QUP 12, lane 2: SPI_SCLK/UART_TX	

2.2.14. Battery interface

Battery interfaces are special for battery interface, major for monitoring battery status, inserting and voltage detection.

Table 2-16. Battery interface definition

Pin name	Pin	Voltage	Type	Description	Notes
BATT_ID	B675	1.875V max	AI	Battery ID input to ADC and MIPI BIF interface. It can be used for missing battery detection	
BATT_THERM	B650	1.875V max	AI	Battery temperature input to ADC for measuring pack temperature. It is used for charger safe operation and BMS/FG.	
VBATT_SNS_M	B750	–	AI	Battery voltage sense input minus	
VBATT_SNS_P	B777	–	AI	Battery voltage sense input plus	
VBATT_PACK_SNS_M	B623	–	AI	Pack sense minus; connected to pack (-) of battery pack	
IBATT_SENSE_M	B673	–	AI	Reserved pin (must be tied to VBATT)	
IBATT_SENSE_P	B700	–	AI	Reserved pin (must be tied to VBATT)	
PMB_DC_IN_EN	A159		DO	DC and wireless charging output enable and disable pin. Keeps the wireless charger output stage disabled (forward voltage blocking) during USB charging	
PMB_DC_IN_PON	B827		AI	DC and wireless charging power-on trigger	
PMB_DC_IN_PSNS	A193		AI	DC and wireless charging input for power sense input	
SMB_THERM	A478		AI	Inductor temperature sensor	

2.2.15. PMICs

The PMICs provide GPIOs and house-keeping pins with different functions.

Table 2-17. PMICs and and GPIOs

PMIC	Pin name	Pin	Voltage	Description	Notes
PM8250	KYPD_HOME_N	B786	1.8	PM8250 GPIO 01 Home key	
	PM_GPIO03_NFC_SLEEP_CLK	B782	1.8	PM8250 GPIO 03 NFC SLEEP_CLK	
	KYPD_VOLUP_N	B761	VPH_PWR	PM8250 GPIO 06 Volumn up key	
	PM_GPIO_07	B755	VPH_PWR	PM8250 GPIO 06	
	PM_GPIO_09	B788	VPH_PWR	PM8250 GPIO 06	
	PM_GPIO_10	B840	VPH_PWR	PM8250 GPIO 10	
PM8150A	PMA_GPIO_01	A277	1.8	spare	
	PMA_GPIO_02	B26	1.8	spare	
	PMA_GPIO_03	A132	1.8	spare	
	PMA_GPIO_04	B99	1.8	spare	
	PMA_GPIO_05	B49	1.8	spare,can act as an AMUX input to the internal ADC	
	PMA_GPIO_06	B126	1.8	spare,can provide a general-purpose PWM via LPG or act as an AMUX input to the internal ADC	
	PMA_GPIO_07	B182	VPH_PWR	Can act as an AMUX input to the internal ADC	
	PMA_GPIO_08	A325	VPH_PWR	spare	
	PMA_GPIO_09	A317	VPH_PWR	spare	
	PMA_GPIO_10	A318	VPH_PWR	spare,can provide a general-purpose PWM via LPG or act as an AMUX input to the internal ADC	
	PMA_GPIO_11	B130	VPH_PWR	spare	
	PMA_GPIO_12	A99	1.8	spare	
	PM8150L_AMUX1	B153	-	Analog multiplexer (AMUX) input 1	AI
	PM8150L_AMUX3	B128	-	Analog multiplexer (AMUX) input 3	AI
PM8150B	PMB_GPIO_01	B775	1.8	PM8150B GPIO 1	
	PMB_GPIO_02	B721	1.8	PM8150B GPIO 2	
	SMB_STAT	B802	VPH_PWR	PM8150B GPIO 6 SMB1355/SMB1390 status	
	PMB_GPIO_07	B798	VPH_PWR	PM8150B GPIO 7	
	PMB_GPIO_08	B773	VPH_PWR	PM8150B GPIO 8	
	PMB_GPIO_10	B800	1.8	PM8150B GPIO 10	
PMR735A	PMR_GPIO_01	A308	VPH_PWR	Spare; can be used as an AMUX input to the internal ADC.	
	PMR_GPIO_02	B4	VPH_PWR	Spare; can be used as an AMUX input to the internal ADC.	
	PMR_GPIO_03	A307	VPH_PWR	Spare; can be used as an AMUX input to the internal ADC.	

2.2.16. LED interface

The SOM provides several LED interfaces, including Flash LEDs, RGB and OLED control signals.

Table 2-18. PWMs and LED Current Driver interface definition

Pin name	Pin	Voltage	Type	Description	Notes
FLASH_LED1	B51,B76		AO	Flash high-side current source for LED1	1.5A max
FLASH_LED2	B24,A130		AO	Flash high-side current source for LED2	1.5A max
FLASH_LED3	B101		AO	Flash high-side current source for LED3	750mA max
PMA_EN_OLEDB	A63		DI	Pin control for OLEDB（OLED Bias)	
PMA_OLED_VREG_ELVDD	A279		PO	Display bias positive: LDO supply power output	
PMA_OLED_VREG_ELVSS	A60		PO	Display bias minus: boost SMPS regulated output	
PMA_OLED_AVDD	A278		PO	OLED LDO power supply output	
RED_LED	A134		AO	RGB LED high-side current source for the red LED	
GREEN_LED	A133		AO	RGB LED high-side current source for the green LED	
BLUE_LED	B78		AO	RGB LED high-side current source for the blue LED	
PMB_HR_LED1	B752		AO	Home row LED current output 1	
PMB_HR_LED2	B725		AO	Home row LED current output 2	

2.2.17. RF interface

The SOM provides fully WLAN and Bluetooth I/F for Wi-Fi+BT module.

Table 2-19. Wi-Fi/BT interface definition

Name	Pin	Description	Notes
SM_UART_HST_BT_CTS_N	B282	GPIO 16 QUP 6, lane 0: SPI_MISO/UART_CTS/I2C_SDA	
SM_UART_HST_BT_RFR_N	B230	GPIO 17 QUP 6, lane 1: SPI_MOSI/UART_RFR/I2C_SCL	
SM_UART_HST_BT_RX	B203	GPIO 19 QUP 6, lane 3: SPI_CS_0/UART_RX	
SM_UART_HST_BT_TX	B151	GPIO 18 QUP 6, lane 2: SPI_SCLK/UART_TX	
SM_UART_HST_BLE_RX	A16	GPIO 177 SSC I/O 17	
SM_UART_HST_BLE_TX	A17	GPIO 176 SSC I/O 16	
SM_SLIMBUS_HST_CLK	B91	GPIO 142 Low-power audio SLIMbus clock MI2S1_SCK	
SM_SLIMBUS_HST_DATA	B143	GPIO 143 Low-power audio SLIMbus data 0 MI2S1_DATA0	
SM_HST_WLAN_EN	B72	GPIO 20	
SM_HST_BT_EN	B124	GPIO 21	Chain0
SM_HST_SW_CTRL	A121	GPIO 124	
SM_UART_HST_WL_RX	A49	GPIO 179 SSC I/O 19	
SM_UART_HST_WL_TX	A50	GPIO 178 SSC I/O 18	

2.2.18. UFS interface

The storage UFS for system is not on SOM. UFS pads are reserved.

Table 2-20. UFS interface definition

Name	Pin	Description	Notes
SM_UFS0_L0_RX_M	A8	UFS 0 receive 0 – minus	
SM_UFS0_L0_RX_P	A7	UFS 0 receive 0 – plus	
SM_UFS0_L0_TX_M	A44	UFS 0 transmit 0 – minus	
SM_UFS0_L0_TX_P	A43	UFS 0 transmit 0 – plus	
SM_UFS0_L1_RX_M	A41	UFS 0 receive 1 – minus	
SM_UFS0_L1_RX_P	A40	UFS 0 receive 1 – plus	
SM_UFS0_L1_TX_M	A10	UFS 0 transmit 1 – minus	
SM_UFS0_L1_TX_P	A11	UFS 0 transmit 1 – plus	
SM_UFS0_REF_CLK	A13	UFS 0 reference clock	
SM_UFS_RST_N	A46	UFS 0 Reset	
SM_UFS1_L0_RX_M	A24	UFS 1 receive 0 – minus	
SM_UFS1_L0_RX_P	A25	UFS 1 receive 0 – plus	
SM_UFS1_L0_TX_M	A22	UFS 1 transmit 0 – minus	
SM_UFS1_L0_TX_P	A21	UFS 1 transmit 0 – plus	
SM_UFS1_REF_CLK	A56	UFS 1 reference clock	

2.2.19. JTAG interface

JTAG signals are designed for software debug purpose.

Table 2-21. JTAG interface definition

Name	Pin	Description	Notes
SM_JTAG_SRST_N	B41	JTAG reset for debug	
SM_JTAG_TCK	B172	JTAG clock input	
SM_JTAG_TDI	B197	JTAG data input	
SM_JTAG_TDO	B145	JTAG data output	
SM_JTAG_TMS	B93	JTAG mode select input	
SM_JTAG_TRST_N	B120	JTAG reset	

2.2.20. Clock interface

SOM provide clocks for different user cases.

Table 2-22. Clock interface definition

Name	Pin	Description	Notes
PMK8002_PMIC_CLK	A445	19.2 MHz clock to the core PMIC or system	
PMK8002_RF_CLK1	B598	38.4 MHz clock	
PMK8002_RF_CLK2	A462	38.4 MHz clock	
PMK8002_RF_CLK3	A453	38.4 MHz clock	
PM_LNBB_CLK2	A142	Typical WCD clock, 19.2MHz	
PM_LNBB_CLK3	A141	Typical NFC clock, 19.2MHz	
PM_RFCLK1	B809	Typical SDR clock, 38.4MHz	
PM_RFCLK2	B834	Typical WLAN clock, 38.4MHz	
PM_RFCLK3	B807	Typical QCA clock, 38.4MHz	
PM_SLEEP_CLK	B709	32 kHz sleep clock to a GPIO of the core PMIC, for further distribution	

2.2.21. Others pins

Pins are not listed above.

Table 2-23. Others pins

Pin name	Pin	Voltage	Function	Notes
SM_GPIO_66	B490	1.8	-	
SM_GPIO_67	B492	1.8	-	
SM_GPIO_68	B440	1.8	GPIO 68 Displayport hot plug detect	
SM_GPIO_69	B682	1.8	GPIO 69 Quad-SPI chip select 0	Other Quad SPI signals are multiplexed with SDC4
SM_GPIO_70	B651	1.8	GPIO 70 Quad-SPI data bit 0	
SM_GPIO_78	B519	1.8	-	
SM_GPIO_88	B690	1.8	-	
SM_GPIO_89	B162	1.8	-	
SM_GPIO_90	B551	1.8	-	
SM_GPIO_109	B201	1.8	-	
SM_GPIO_110	A122	1.8	-	
SM_GPIO_111	A53	1.8	-	
SM_IMU2_INT	B16	1.8	GPIO 112	
SM_MAG_INT_N	B68	1.8	GPIO 113	
SM_GPIO_114	A87	1.8	-	
PM_PS_HOLD	B738	1.8	Power supply hold signal from QRB5165N to PMIC	
PMA_DISP_SCTRL	A97	1.8	Hardware SWIRE interface AMOLED displays	
FLASH_STROBE	A131	-	Digital input for flash strobe signal	
PMB_AMUX1_WP_THERM	A470	0~1.875	nput for skin and remote thermistor sense.	AMUX_1 of PM8150B
PMB_HOUT_M	B698		Haptics H-bridge driver output minus	Peak drive voltage 5V with external boost
PMB_HOUT_P	B723		Haptics H-bridge driver output plus	
CBL_PWR_N	B842		Cable power-on ground switch (200 kΩ internal PU to 1.8 V)	
MDM_SKIN_THERM	B784	0~1.875	Analog multiplexer (AMUX) input 1; MSM thermistor	AMUX_1 of PM8250
WIFI_SKIN_THERM	B838	0~1.875	Analog multiplexer (AMUX) input 2; UFS therm	AMUX_2 of PM8250
SM_RESIN_N	B713	-	Reset output to SM8150/SM8250 device's RESIN_N	
SM_RESOUT_N	B794	1.8	Reset output of QRB5165N	
ISNS_SMB_P	A461	-	Current sense plus from external parallel charger	
ISNS_SMB_M	A469	-	Current sense minus from external parallel charger	
SMB_EN_CHG	B748	-	Enable and disable control pin for the dual slave (SMB) charger.	
USBC_CONN_THRM	B648	-	USB Type-C connector temperature sensor	
PMIC_SPMI_CLK	A471	-	SPMI communication bus clock signal	
PMIC_SPMI_DATA	A479	-	SPMI communication bus data signal	
PM_FAULT_N	B54	1.8	To send/receive the fault condition across all PMICs.	Internal 200 Kohm pull up to 1.8V.

Chapter 3. Electrical Characteristics

3.1. Absolute maximum ratings

The SOM needs to be designed in the operation conditions shown in the table below.

Table 3-1. Absolute rating condition

Parameter	Min	Max	Units
Input Power Voltage			
USB_VBUS	-0.3	28	V
VBAT	-0.3	6	V
VBATT_SNS_P, VBATT_SNS_M	-0.3	6	V
ESD			
ESD-HBM model rating		±1000	V
ESD-CDM model rating		±250	V

➲ **NOTE:** for the ESD, it will be valid and available only when the module is fully tested and approved in the Initial Production stage.

3.2. Operating conditions

The SOM needs to be designed in the operation conditons which is shown as below table.

Table 3-2. Operating conditions

Parameters	Min	Typical	Max	Units
Input Power voltage				
USB_VBUS	+3.6	5	+13.2	V
VBAT	+3.4	3.8	+4.35	V
VBAT	3			A
VBATT_SNS_P, VBATT_SNS_M,	+3.4	3.8	+4.35	V
Thermal conditions				
Operating temperature	-25	25	75	°C
Storage temperature	-40	-	TBD	°C

➲ **NOTE:** The min and max operating temperatures specified in the above table shall not exceed those of relevant IC (see Table 3-3).

Table 3-3. IC Temperature

Chipset	Thermal Condition (min, °C)	Thermal Condition (max, °C)
QRB5165N	Ta=-40	Tj=115
PM8250	Ta=-30	Tj=95
PM8150B	Tc=-30	Tc=85
PM8150A	Ta=-30	Ta=85
PMR735A	Tj=-30	Tj=125
PMK8002	Tj=-35	Tj=115
LPDDR	Ta=-25	Ta=85

➲ **NOTE:**

- Ta: a=ambient, temperature of the working environment.
- Tc: c=case, *surface temperature*, which can be simply understood as ambient temperature + CPU temperature rise. Generally speaking, Tc is slightly higher than the ambient temperature.
- Tj: j=junction, *junction temperature*, which can be simply understood as the chip internal temperature.

3.3. Output power

The SOM provide power supply for external device, like camera module, SD card, sensor, and so on.

Table 3-4. Output power

Pin name	Default voltage(V)	Active Range	Default state/ boot voltage	Rated current* (mA)	Source Regulator
VCOIN	3.0	2.0~3.25	-	-	VPH_PWR
VREG_BOB	3.3	3.0~4.0	3.3	1500	VPH_PWR
VREG_L2A_3P07	3.072	3.072	3.072	50	VREG_BOB
VREG_L6A_1P2	1.2	1.2	1.2	700	VREG_S8C_1P3
VREG_L7A_1P7	1.704	-	-	600	S5A
VREG_L12A_1P8	1.8	1.8	1.8	-	S5A
VREG_L14A_1P8	1.8	1.8	-	300	S5A
VREG_L15A_1P8	1.704	1.704	-	600	S5A
VREG_L16A_3P3	3.024	-	-	300	VREG_BOB
VREG_L17A_2P96	3.008	2.856~3.008	-	600	VREG_BOB
VREG_S4A_1P8	1.8	1.8	1.8	900	VPH_PWR
VREG_S5A_1P9	1.952	1.81~2.04	1.952	600	VPH_PWR
VREG_S6A_0P9	0.952	0.93~1.1	0.952	150	VPH_PWR
VREG_L1C_1P8	1.8	1.8	-	150	S4A
VREG_L2C_1P3	1.304	1.304	-	400	S8C
VREG_L3C_0P8	1.2	1.2	-	400	S8C
VREG_L4C_1P8	1.808	1.704~2.928	-	150	VREG_BOB
VREG_L5C_1P8	1.808	1.808	-	150	VREG_BOB
VREG_L7C_2P8	3.008	2.856~3.104	-	400	VREG_BOB
VREG_L8C_1P8	1.8	1.8	-	150	S4A
VREG_L9C_2P9	2.96	2.704~2.96	2.96	600	VREG_BOB
VREG_L10C_3P0	3.312	3.312	-	400	VREG_BOB
VREG_L11C_3P3	3.104	3.0~3.312	-	400	VREG_BOB

Pin name	Default voltage(V)	Active Range	Default state/ boot voltage	Rated current* (mA)	Source Regulator
VREG_S8C_1P3	1.352	1.27~1.352	1.352	600	VPH_PWR
PMR_VREG_L1	0.88	0.88	-	600	VREG_S8C_1P3
PMR_VREG_L2	1.2	1.2	-	600	VREG_S8C_1P3
PMR_VREG_L3	1.2	1.2	-	600	VREG_S8C_1P3
PMR_VREG_L4	1.776	1.776	-	400	VREG_S5A_1P9
PMR_VREG_L5	0.8	0.8	-	600	VREG_S8C_1P3
PMR_VREG_L6	0.8	0.72~0.824	-	600	VREG_S8C_1P3
PMR_VREG_L7	2.8	2.8	-	150	VREG_BOG
PMR_VREG_S3G_2P2	2.2	2.2	-	1500	VPH_PWR

*: Rated current, excluding current consumption of power rails in the above table.

3.4. Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage. The SOM IO voltage level is the same with VDDPX_3 except the SD card and analog input/output. The I2C, USB, MIPI and UART comply with the standards.

3.4.1. Digital GPIO characteristics

The follow-int table shows the digital GPIO characteristics:

Table 3-5. Digital IO voltage performance

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt	0.7 x VDDPX_3	VDDPX_3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt	-0.3	0.3 x VDDPX_3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

3.4.2. SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.96V. The following table shows the SD card digital I/O characteristics.

Table 3-6. SD digital IO voltage performance (1.8V/2.96V)

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/0.625 x VDDPX_2	-	2/VDDPX_2 + 0.3	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.58/0.25 x VDDPX_2	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω

RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/0.75 x VDDPX_2	-	-/VDDPX_2	V
VOL	Low-level output voltage	0/0	-	0.45/0.125 x VDDPX_2	V

3.5. MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Table 3-7. MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

Table 3-8. MIPI_CSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 is not supported; DPCM 2 is not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.2	None

3.6. USB

The SOM supports USB standards and exceptions.

Table 3-9. USB

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2

3.7. PCIe

The SOM supports PCIe standards and exceptions

Table 3-10. PCIe

Applicable standard	Feature exceptions
PCI Express Specification, Revision 3.0	Gen3

3.8. DisplayPort

The SOM supports DisplayPort standards and exceptions

Table 3-11. DP

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	HBR3

3.9. SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Table 3-12. SLIMbus

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.10. SDIO

The SOM Supports SD standards and exceptions

Table 3-13. SDIO

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

3.11. I2S

The SOM I2S standards and exceptions:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions.

It supports the following functions:

- Both master and slave mode
- 16, 24, or 32-bit resolution audio samples
- 8, 16, 32, 48, 96 and192 kHz sampling rate in Master mode, and all standard sample rates in slave mode.
- 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s)

Maximum clock frequency supported 12.288 MHz.

An additional Pin can be used for a master clock, supplied by the MSM device, the master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Table 3-14. I2S

Applicable standard	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	None

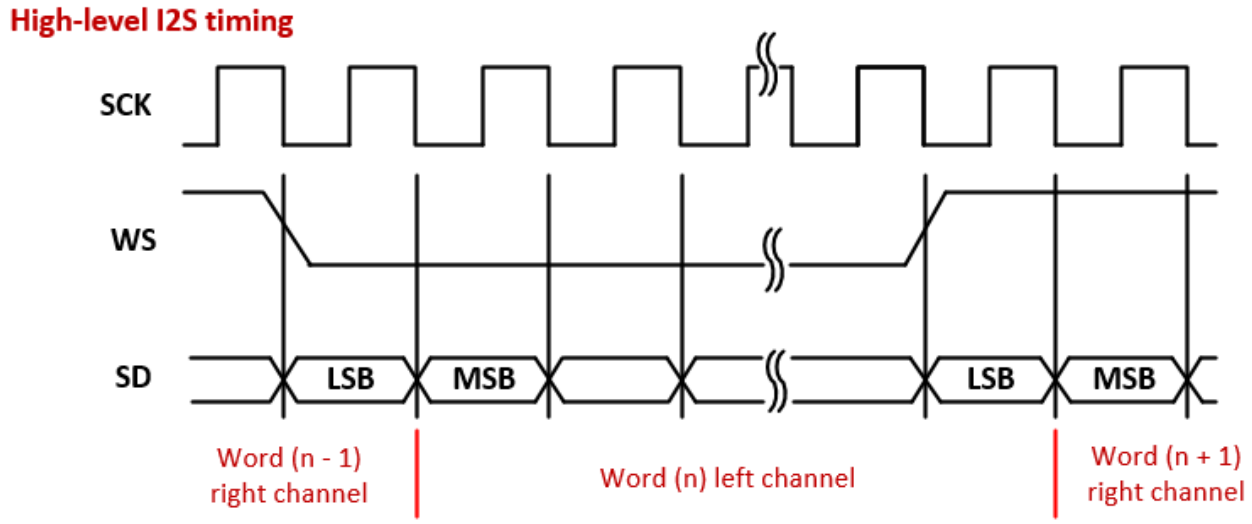


Figure 3-1.I2S Timing Diagram

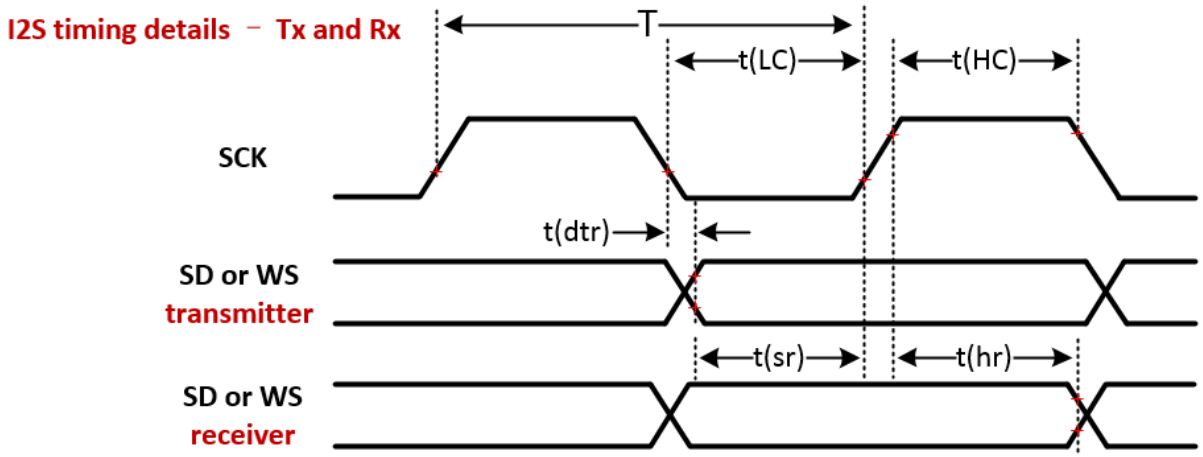


Figure 3-2.I2S Timing Diagram

The word-select signal is a 50% duty cycle signal Data is delayed 1 bit-clock, relative to the word select.

Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.

I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.

The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high.

Table 3-15. I2S Timing

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns

3.12. I2C

The SOM I2C standards and exceptions:

Table 3-16. I2C

Applicable standard	Feature exceptions
I2C Specification, version 3.0	TBD

3.13. SPI

The SOM supports SPI standards as a master only.

3.14. Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the Battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.

Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

Table 3-17. Fuel Gauge

Function	Min	Type	Max	Units	Expected use
VBATT_SNS_P (B777) & VBATT_SNS_M(B750)					
Resolution	-	-	16	bits	Voltage ADC
	1	-	450	Kohm	ID ADC
	-	-	16	bits	Current ADC

3.15. Power consumption

T.B.D.

3.16. Thermal

T.B.D.

3.17. RF Performance

T.B.D.

Appendix 1. Notices

Thundercomm may have patents or pending patent programs covering subject matter described in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries to service@thundercomm.com.

THUNDERCOMM PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some jurisdictions do not allow disclaimer of express or implied warranties in certain transactions; therefore, this statement may not apply to you.

Changes are made periodically to the information herein; these changes will be incorporated in new editions of the publication. To provide better service, Thundercomm reserves the right to improve and/or modify the products and software programs described in the manuals, and the content of the manual, at any time without additional notice.

The software interface and function and hardware configuration described in the manuals included with your development board or system on module might not match exactly the actual configuration of that you have purchased. For the configuration of the product, refer to the related contract (if any) or product packing list, or consult the distributor for the product sales. Thundercomm may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation to you.

The products described in this document are not intended for use in implantation or other life support applications where malfunction may result in injury or death to persons. The information contained in this document does not affect or change Thundercomm product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of Thundercomm or third parties. All information contained in this document was obtained in specific environments and is presented as an illustration. The result obtained in other operating environments may vary.

The information of this document should not be as any invitation for offer or any advice to the visitors. Please consult the professional comments from the sales consultant prior to do any actions of invest or purchase.

Thundercomm may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation to you.

Any references in this publication to non-Thundercomm Web sites are provided for convenience only and do not in any manner serve as an endorsement of those Web sites. The materials at those Web sites are not part of the materials for this Thundercomm product, and use of those Web sites is at your own risk. Thundercomm shall not be responsible for the content of the third party.

Any performance data contained herein was determined in a controlled environment. Therefore, the result obtained in other operating environments may vary significantly. Some measurements may have been made on development-level systems and there is no guarantee that these measurements will be the same on generally available systems. Furthermore, some measurements may have been estimated through extrapolation. Actual results may vary. Users of this document should verify the applicable data for their specific environment.

E-mail messages sent to Thundercomm via the Internet are not guaranteed to be completely secure. Thundercomm shall not be liable for any loss incurred by the surfer when transmitting any information over the Internet or for any loss incurred by Thundercomm when sending any information over the Internet at your request.

Thundercomm has all rights under other relevant exemptions provided by laws and regulations, and Thundercomm's failure to claim or delay in claiming such rights shall not be deemed to be a waiver of such rights by Thundercomm.

Thundercomm reserves the right of final interpretation of this document.

Appendix 2. Trademarks

Thundercomm, Thundercomm TurboX, TURBOX, Thundersoft turbox are trademarks of Thundercomm Corporation or its associate companies in China and/or other countries. Intel, Intel SpeedStep, Optane, and Thunderbolt are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Microsoft, Windows, Direct3D, BitLocker, and Cortana are trademarks of the Microsoft group of companies. Mini DisplayPort (mDP), DisplayPort, and VESA are trademarks of the Video Electronics Standards Association. The terms HDMI and HDMI High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries. Wi-Fi, Wi-Fi Alliance, WiGig, and Miracast are registered trademarks of Wi-Fi Alliance. USB-C is a registered trademark of USB Implementers Forum. All other trademarks are the property of their respective owners.