Jan 16, 2023

Snapdragon digital chassis

SNAPDRAGON RIDE PLATFORM

Qualcomm Technologies, Inc.

Image: Qualcomm Concept Vehicle - CES2023 Las Vegas

SNAPDRAGON RIDE PLATFORM - SOC LINEUP

Snapdragon Ride: A comprehensive solution for advanced driver assistance and autonomous driving

Drive Policy	→	Qualcomm Arriver, BMW
Front and surround vision	→	Qualcomm Arriver
Maps	→	Qualcomm, here, TomTom
Parking	→	Pre-integrated partner: Valeo, Bosch, ZongMu or OEM
Driver monitoring	→	Pre-integrated partner: seeingmachines or OEM
Ride SDK: Middleware, Tools & Libraries	→	Qualcomm
Safe OS | Drivers | Hypervisors	→	Qualcomm, QNX, Red Hat

Sensors:

• APTIV • BOSCH Continental onsemi SAMSUNG SONY veoneer

Snapdragon® Vision SoC

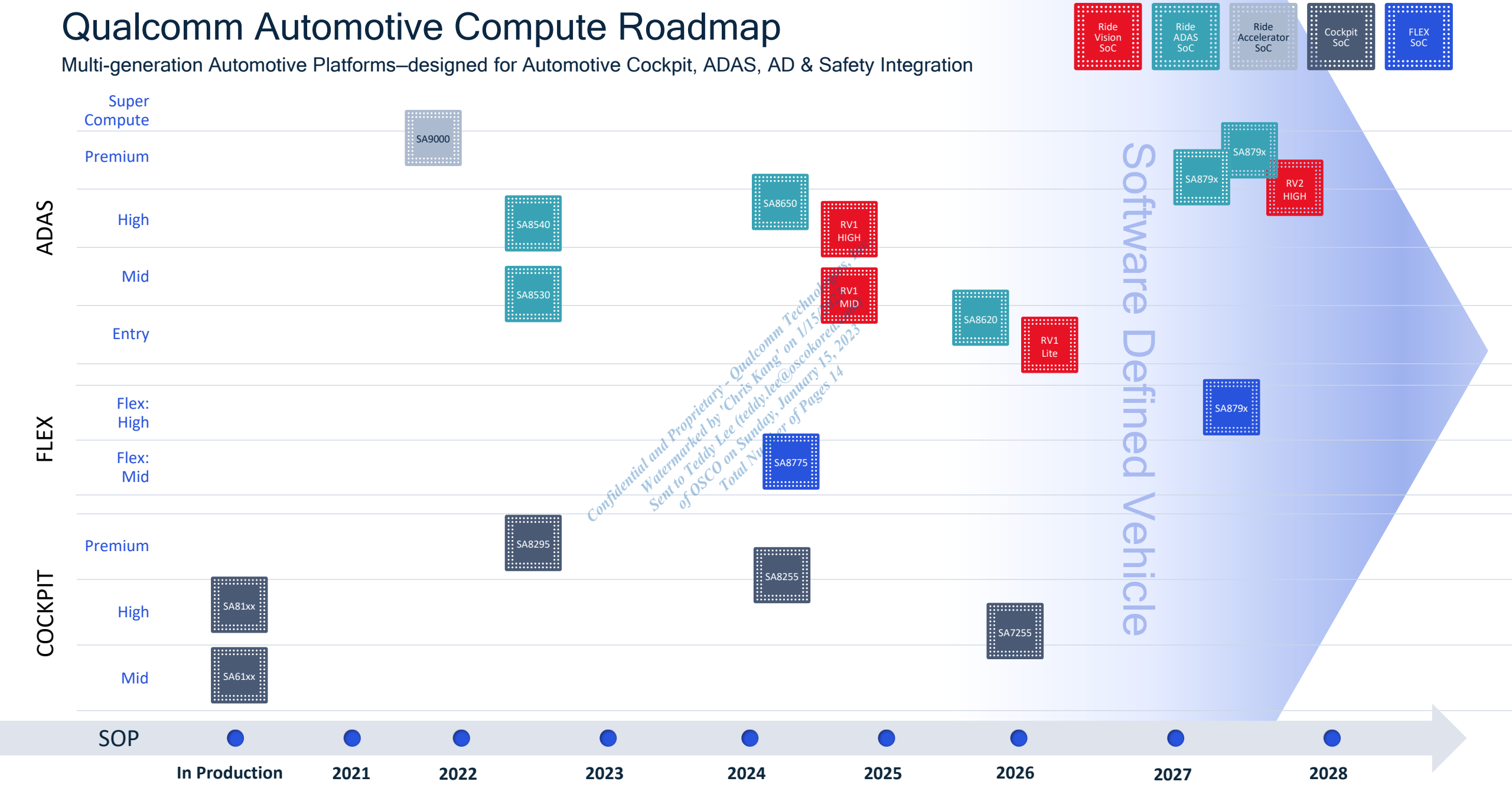
Snapdragon® Ride SoC
Scalable L1 to L3 Ride SoCs

Snapdragon® Accelerator
L3/L4 ADAS Accelerator

Snapdragon ride platform

Qualcomm Automotive Compute Roadmap

Multi-generation Automotive Platforms–designed for Automotive Cockpit, ADAS, AD & Safety Integration

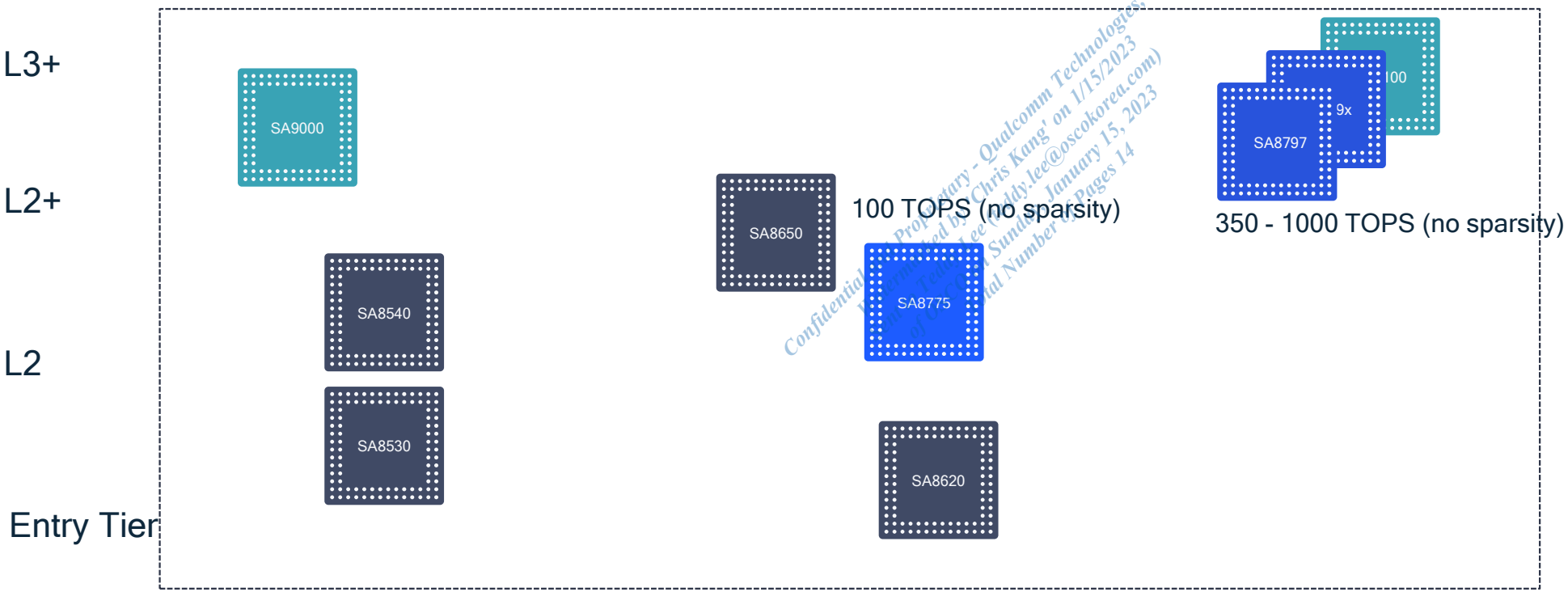


Industry leading & broadest compute portfolio

Scalable and Cross-functional Compute Roadmap designed for Software Defined Central Compute

RIDE ADAS SOC | RIDE ACCELERATOR SOC | FUSION SOC

- 24 to 2000+ TOP scalability
- High efficiency CPU cores & Safe GP-GPU
- ASILB & ASIL D compute integration
- Best in class power, performance and functional safety
- Software scalability and comprehensive tools



Turn-key prototyping reference designs available w/ SW and optimized cooling solutions

Ride 3.0

Ride 4.0

SOP — In Production — 2024 — 2025 — 2026 — 2027

Automotive ADAS SOC family and SKUs

		ADAS SOCs		Accelerators
		SA8650P	SA8620P	SA9000P-xxxx
COMPUTE	Main CPU Type / count / DMIPs	8x Core Kryo Gen6 **up to 230k DMIPs**	4x Core Kryo Gen6 **up to 100k DMIPs**	Quad Cortex A53 for control of ML engines
	RT CPU Type / count / DMIPs (this is part of safety island / SMSS)	4x Core Cortex R52 **up to 18k split / 8k lockstep ASIL D**	4x Core Cortex R52 **up to 16k split / 7k lockstep ASIL D**	-
	NSP count / TOPs	2x NSP **up to 100 TOPs (Int8)**	1x NSP **up to 36 TOPs (Int8)**	14x NSP **up to 300 TOPs (Int8)**
	GPU Type / GFLOPs	A663 **up to 1300 GFLOPs**	A66x **up to 400 GFLOPs**	-
Memory	DDR Config	6x16 **Up to 77 GB/s**	4x16 **Up to 52 GB/s**	**Up to 130+ GB/s** Inline ECC
	On chip SRAM	**20MB+** distributed between CPU, NSP, GPU, SAIL etc	**10MB+** distributed between CPU, NSP, GPU, SAIL etc	**100MB+** distributed between NSP
HWAs	Video Encode / Decode	**up to 4k120/4k120**	**up to 4k60/4K60**	-
	ISP support	**Upto 2GP/s**	**>1GP/s**	-
	Dense optical Flow	**240 MP/s**	**120 MP/s**	-
	IO Peripherals, Safety specifications	Refer to detailed spec table		
	Package	**SIP**	**COB or SIP**	**SIP**

*- DMIPS is not an estimate of true performance. Estimated only and subject to compiler options
**- GFLOPS is not an estimate of true performance. Turbo mode for GPU assumed. Sustained GFLOPS will be lower

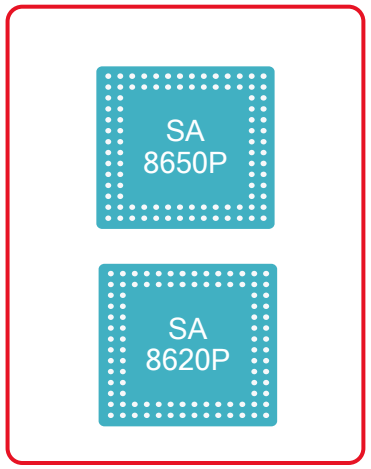
Automotive ADAS SoC Peripheral Specifications

Chipset	SA8650P	SA8620P
Camera Ports	4x 4L CSI2.0 ports w/ CPHY and DPHY support	3x 4L CSI2.0 ports w/ CPHY and DPHY support
PCIe support	6 Lanes -1x4 + 1x2 (Gen4)	2 Lanes 1x2 (Gen4)
Ethernet support	2x 2.5GbE w/ TSN (2 x SGMII) 1x 1GbE RGMII (in safety island)	1x 2.5GbE w/ TSN (1x SGMII) 1x 1GbE RGMII (in safety island)
USB support	2x USB 3.1	1x USB 3.1
Storage i/f support	2xUFS 3.1 G4 2lanes, OSPI, NVMe over PCIe	1xUFS 3.1 G4 2lanes, OSPI, NVMe over PCIe
Audio Support	-	-
CAN-FD	6x CAN-FD	6x CAN-FD
Other Peripherals	1x SDIO, 15 Serial Interfaces, 175+GPIOs	1x SDIO, 10 Serial Interfaces, 100+GPIOs
Package	25x25 FCBGA, 0.6 mm pitch	25x25 FCBGA, 0.6 mm pitch
Safety Support	Integrated Safety Island - ASIL -D SOC - ASIL-B	Integrated Safety Island - ASIL -D SOC - ASIL-B
Power Consumption* (TDP70 typical - Corner Parts)	~35 - 42W	~18 - 25W

Snapdragon Automotive ADAS Chipsets

Targets under execution, subject to potential change

Target specifications & schedule



SA8650P	X	X	X	X
	CPU	GPU	ML / AI	DDR
A	230K	Up to 1.3 TFLOPS	100 TOPS	DDR - 77 GB/s
B	200K	Up to 1.0 TFLOPS	72 TOPS	DDR - 52 GB/s
C	180K		50 TOPS	

SA8620P	X	X	X	X
	CPU	GPU	ML / AI	DDR
A	100k	Up to 0.4 TFLOPs	36 TOPs	DDR - 52 GB/s

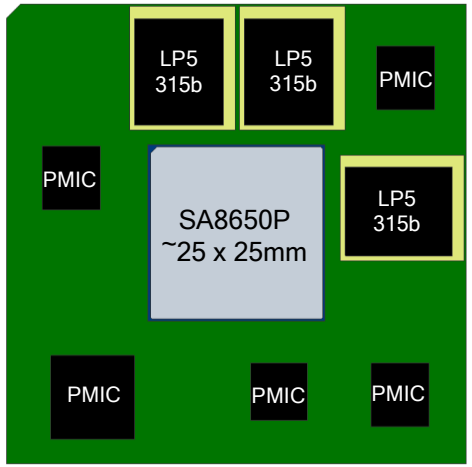
*SA85xP & SA9000x platforms for Development – **Available Now***

Milestones	SA85x0P-xxxx	SA8650P-xxxx	SA8620P-xxxx	SA90xxP-xx
Early Prototyping Samples	Available Now	Available Now (using SA8650P SIP)		Available Now
Early SIP Samples	Available Now	Oct 2022	Aug 2023	Available Now
Qualification Complete Samples	Available Now	Feb 2024	Dec 2024	Available Now

QAM8650P Module Design Attributes (preliminary)

For early development, use QAM8540P as reference and discuss with Qualcomm for detailed review

Module	
Package Type	BGA Module
Package Size	65x65 mm
Mold Cap	NA
Module Thermal Lid	NA
Total Height	TBD max
BGA Pitch	1.27 mm
BGA SRO	630 um
Mainboard Pad	630 um (NSMD)
BGA Alloy	SAC305
BGA Count	1573
Shielding	No
Underfilled Component	DRAM



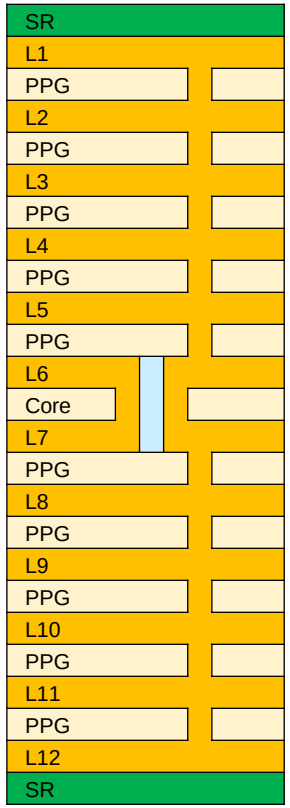
Floor Plan (Preliminary)

Component Details	
APQ	SA8650P Qty: 1
	25x25mm FCBGA
LPDDR5	Auto Grade Qty: 3
	Qty: 2 12.4x15 0.7 pitch
PMIC	Design scoping in progress
Components	Design scoping in progress
Components Count	Top Side: ~250 BGA Side: ~100 0201 Total: ~350
Tallest Component	SoC FCBGA

Assembly Materials	
Solder paste	SAC305
BGA UF	Non-reworkable

Dimensions: 65x65mm

Substrate	
Substrate Technology	HDI
Substrate Stackup	5-2-5
Layer Count	12 L
PCB Thickness	1.6 mm



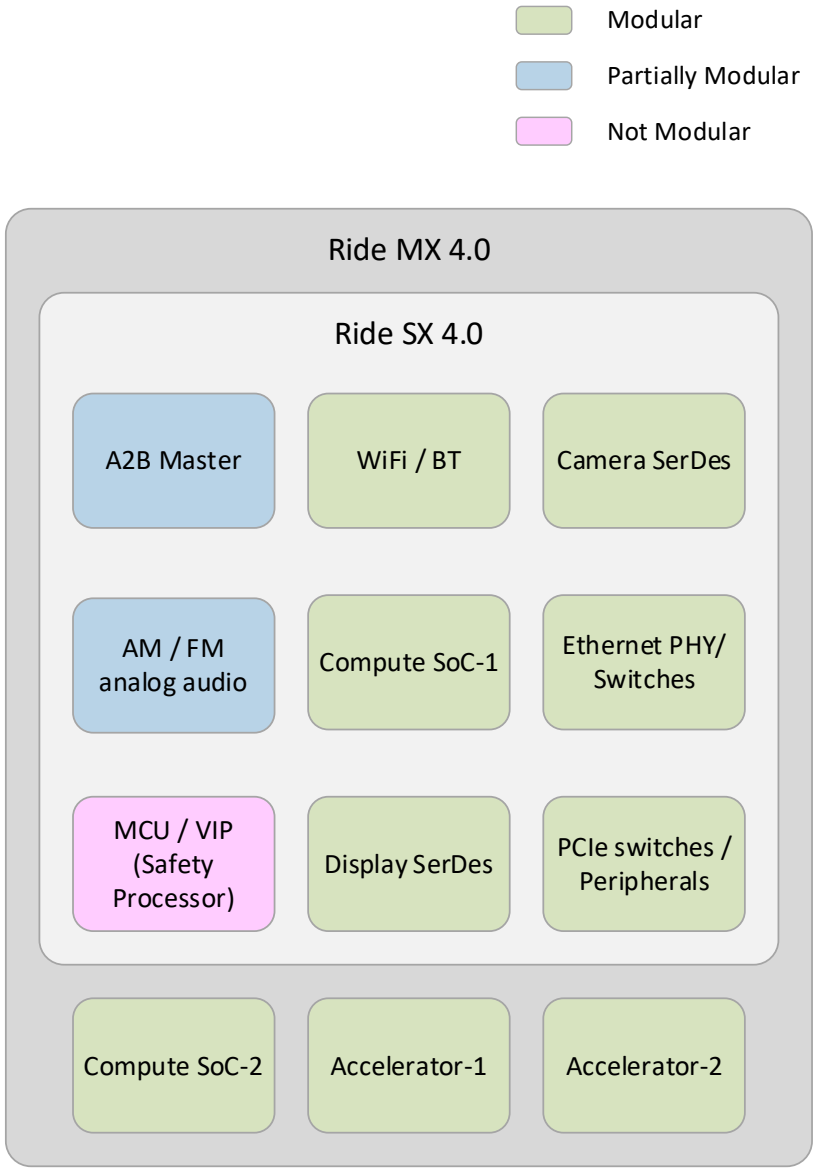
Qualcomm Reference Design Board - Ride 4.0 HW Platform

Ride 4.0 Platforms

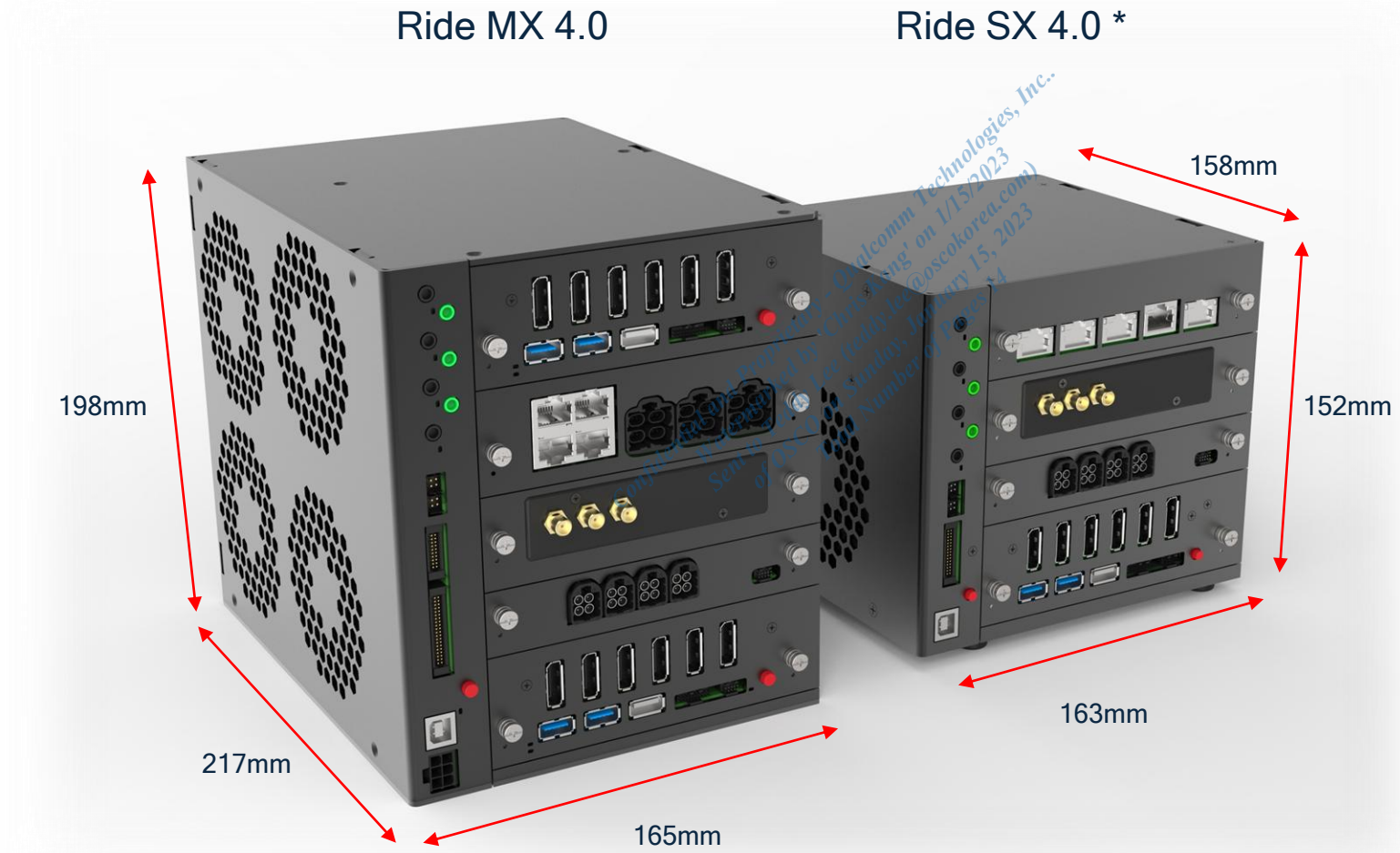
- 2 Platforms in the Ride 4.0 family
  - **Ride SX** – Single-SoC Platform (*previously referred to as ADP-AIR*)
  - **Ride MX** – Mult-SoCs Platform

- Both Platforms share a common architecture and several pluggable cards

- Highly modular, can be adapted to several different use cases. Modules include:
  - Camera SerDes
  - Display SerDes
  - PCIe Switch and peripherals
  - Ethernet Switches, PHYs and Peripherals
  - Audio devices (On the Ride SX)



Ride 4.0 Hardware Platforms

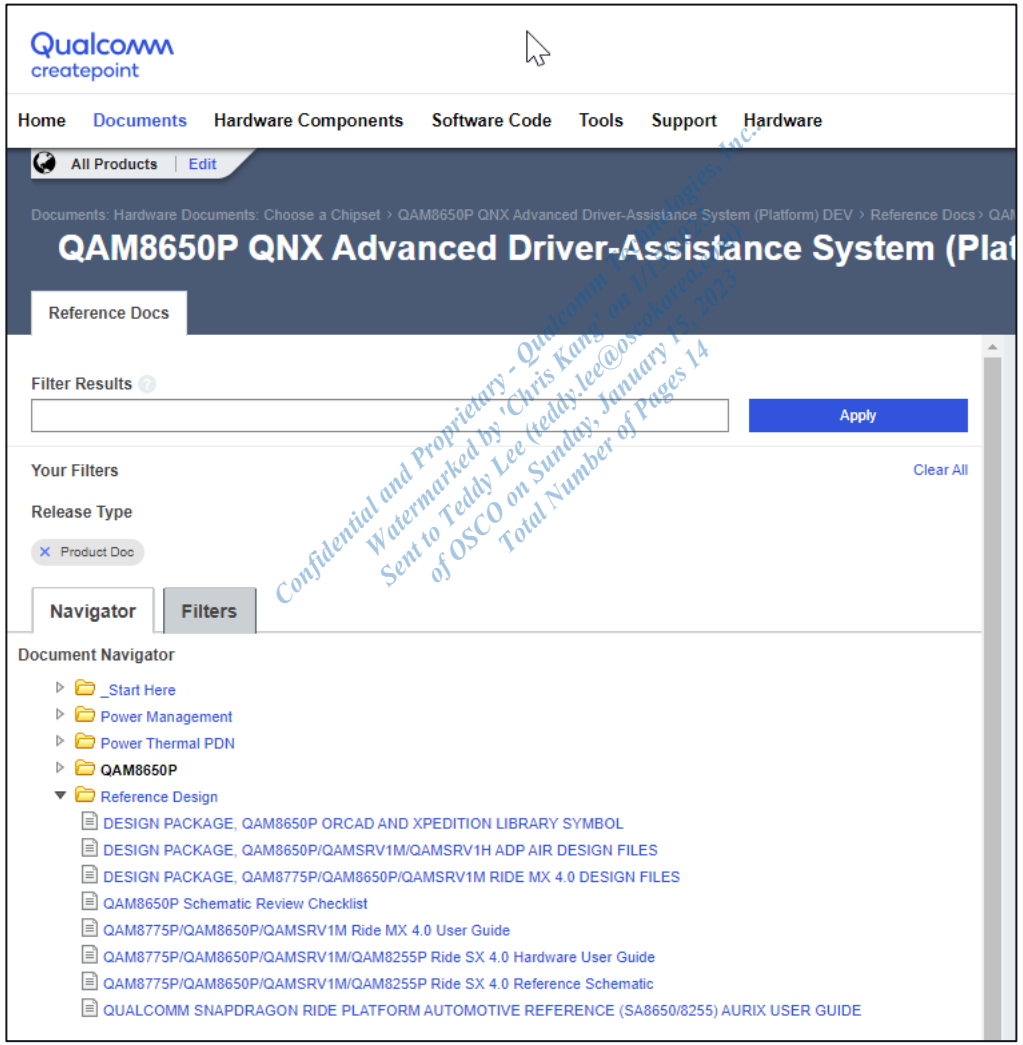


** NOTE: Ride SX 4.0 is the same platform which was previously called ADP-AIR*

Preliminary Information. Design is in progress and some details may change

Qualcomm Createpoint - https://createpoint.qti.qualcomm.com/

- Example : DCN 80-31747-700 **QAM8650P (SA8650P SIP) Announcement and Documentation**



Thank you

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