Qualcomm Technologies, Inc.

QAM8295P

ADP Star User Guide

80-PU692-123 Rev. AC

February 10, 2023

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Revision history

Revision	Date	Description
AA	February 2021	Initial release
AB	May 2021	▪ Table 1-1 QAM8295P automotive development platform references: Updated the title of the table ▪ Section 2.1 QAM8295P overview: Updated the section ▪ Table 2-2 QAM8295P feature set summary: ▫ Updated the title of the table ▫ Updated the table and added a table footnote ▪ Section 2.2 QAM8295P/SA8295P key features and interfaces: Deleted the note ▪ Figure 3-1 SA8295P/QAM8295P validation platform: Updated the figure ▪ Table 3-1 Board summary: Updated the table ▪ Section 3.1 Board summary of auto validation platform: Added the note ▪ Section 3.2 Ports and interfaces: ▫ Table 3-2 Power and JTAG connector details in ADP STAR platform: Updated the table ▫ Added a note ▪ Figure 3-6 ADP STAR board architecture with QAM8295P: Updated the figure ▪ Section 4.1 Main board architecture: Updated the section with peripheral card information ▪ Figure 4-1 ADP STAR power tree: Updated the figure ▪ Section 4.8 PCIe (OCuLink) overview: Updated the section ▪ Table 4-9 PCIe interface connectors: Added the table ▪ Section 5 VIP (AURIX) daughtercard (PR898): Updated the section ▪ Section 6 Ethernet daughtercard (PW188): Updated the section ▪ Section 7 BRAC daughtercard (PT121): Updated the section ▪ Section 8 Camera daughtercard (PW171): Updated the section ▪ Section 9 Flash memory daughtercard (PT120): Updated the section ▪ Removed the section 10 ordering guide
AC	February 2023	▪ Figure 5-3 *VIP (AURIX) block diagram*: Updated the note.

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1 Introduction

1.1 Purpose

This document provides a high-level summary of the Automotive validation platform with the Qualcomm® Snapdragon™ SA8295P/QAM8295P chipset and provides a start-up guidance.

1.2 Scope

The scope of the document is to provide high-level details of the system block diagrams, electrical design, features, and capabilities of the platform.

1.3 References

Additional technical information on the SA8295P/QAM8295P automotive chipset is provided and covered by the documents listed in Table 1-1. The documents are available from the Qualcomm® CreatePoint website at https://createpoint.qti.qualcomm.com.

Table 1-1 QAM8295P automotive development platform references

DCN	Title/description
80-PU692-1	*QAM8295P Data Sheet*
80-PU692-1A	*QAM8295P Pin Assignment and GPIO configuration Spreadsheet*
80-PU692-5A	*QAM8295P Chipset Introduction*
80-PU692-5B	*QAM8295P Design Guidelines/Training Slides*

2 Overview

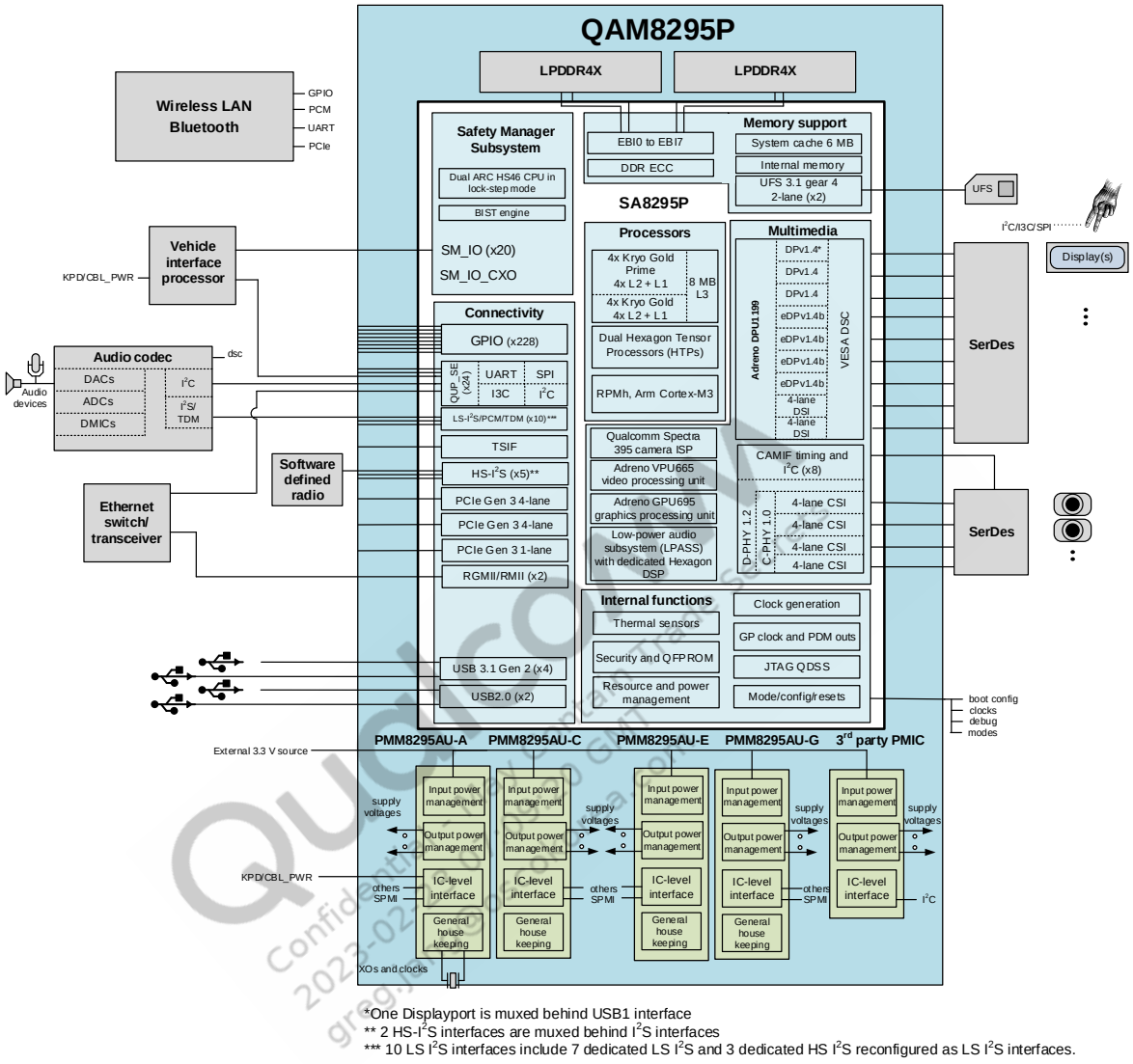
2.1 QAM8295P overview

- QAM8295P is the next generation Qualcomm® Snapdragon™ automotive infotainment module designed for superior performance and power efficiency. It has been developed as an SEooC (Safety element out of context) targeting assumed ASIL B use cases. The key components of the QAM8295P module include SA8295P SoC, four instances of PMM8295AU power management IC, one third party power management IC, and two 556-ball LPDDR4X SDRAM.
- SA8295P includes the following key components:
  Qualcomm® Kryo™ 695 CPU built on Arm v8 Cortex technology, Qualcomm® Adreno™ 69x GPU, Dual Qualcomm® Hexagon™ Tensor Processors, Qualcomm Spectra™ ISP 395, Adreno 665 VPU, Adreno DPU 1199, and dedicated Safety manager subsystem.

Table 2-1 Key features and interfaces

Feature	SA8295P
Package	25 mm × 25 mm × 2.25 mm FCBGA + HS
CPU	▪ Qualcomm® Kryo™ 695, 8 MB L3 ▪ 4 × Gold prime core up to 2.688 GHz ▪ 4 × Gold cores up to 2.438 GHz
Memory	8 × 16 LPDDR4X; up to 2092.8 MHz
GPU	Qualcomm® Adreno™ 695
AI/NSP	V68, 4 × Qualcomm® Hexagon™ Vector eXtensions (HVX), 2 × HMX, up to 1.4 GHz
Display	Adreno DPU 1199, 64 MP, DSC v1.2, up to 600 MHz
Camera	Qualcomm Spectra™ 395, 2.5 Gbps/lane, 40 Gbps total
Video	Adreno VPU 665, decode 4k240, encode 4k120, concurrent 4k120 decode/encode
Audio	V66 2 MB L2 up to 1.459 GHz
Functional safety	Safety Element out of Context (SEooC) targeting assumed ASIL B use cases. Contains dedicated Safety Manager sub-system, with lock step core
Junction temp	-40°C to +115°C

NOTE: This is not a comprehensive or controlling list of chipset features; See the *QAM8295P Data Sheet* (80-PU692-1) and *QAM8295P Design Guidelines* (80-PU692-5B) for more details.



*One Displayport is muxed behind USB1 interface
** 2 HS-I²S interfaces are muxed behind I²S interfaces
*** 10 LS I²S interfaces include 7 dedicated LS I²S and 3 dedicated HS I²S reconfigured as LS I²S interfaces.

Figure 2-1 QAM8295P functional block diagram

Major architectural blocks:
1. Kryo subsystem (CPUSS)
2. Always-on subsystem (AOSS)
3. Multimedia subsystem (MMSS)
4. Low-power audio subsystem (LPASS)
5. Peripheral subsystem (PSS)
6. Safety Manager subsystem (SMSS)
7. Secondary Serial Cluster subsystem
8. Memory support and the bus system that supports all major blocks
9. Hexagon Tensor Processor Subsystem (HTPSS)

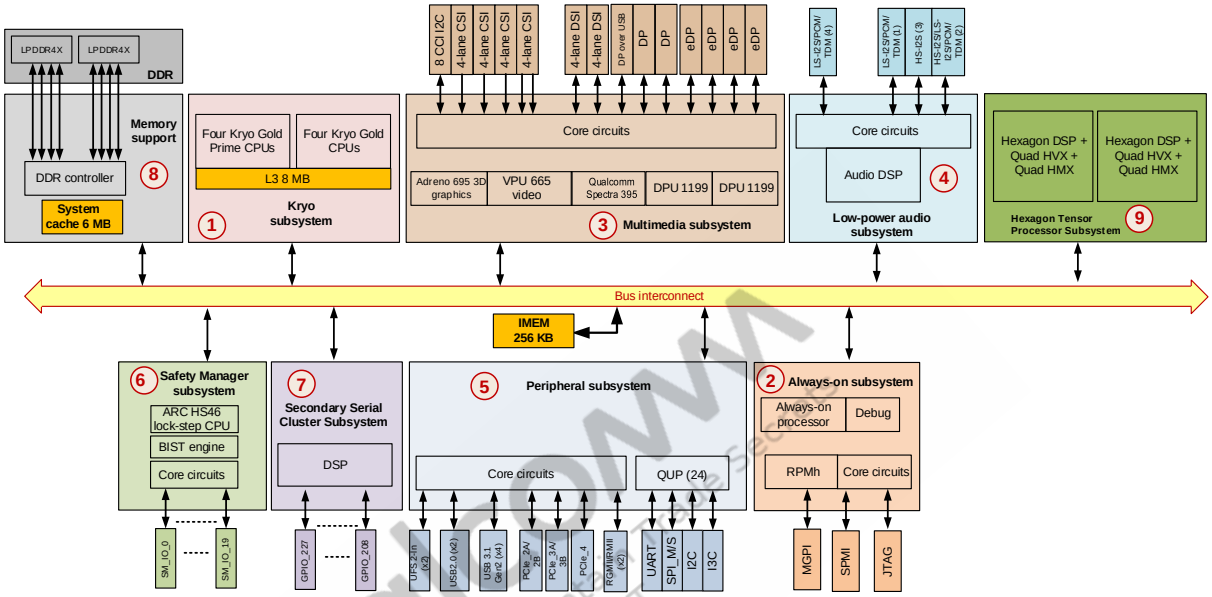


Figure 2-2 SA8295P architecture overview

2.2 QAM8295P/SA8295P key features and interfaces

Table 2-2 QAM8295P feature set summary

Feature	QAM8295P
Display DisplayPort/eDP	Three 4-lane DisplayPort v1.4, One DisplayPort shared with USB 3.1 Gen 2 Four 4-lane embedded DisplayPort v1.4b
Display – DSI	DSI D-PHY v1.2 4-lane DSI0 4-lane DSI1
Camera – CSI CCI-I^{2}C	CSI-2 v1.3 4-lane CSI0, 4-lane CSI1, 4-lane CSI2, 4-lane CSI3
Audio – LS- I^{2}S (muxed with PCM/TDM pins)	▪ Up to 10 (7 + 3 *) interfaces (pin multiplexed with PCM/TDM interfaces) ▫ Nine (6 + 3 *) interfaces with two data lanes each 2-data lanes each ▫ One interface with four data lanes for a total of 22 (16 + 6 *) data lanes
Audio – HS-I^{2}S	Five high-speed (up to 73.728 MHz) receive interfaces for software defined radio (SDR); two of them are muxed behind LS- I^{2}S interfaces; all of them can be configured as LS- I^{2}S interfaces if needed
Audio – TDM/PCM muxed with LS- I^{2}S pins	▪ Up to 10 (7+ 3 *) interfaces (pin multiplexed with I^{2}S ▫ Nine (6 + 3 *) interfaces with two data lanes each ▫ One interface with four data lanes
Storage – UFS	Two 2-lane UFS 3.1 gear 4 rate B
PCIe	One 1-lane PCIe 3 (RC/EP) Two 4-lane PCIe 3 (RC/EP)

Feature	QAM8295P
Ethernet – RGMII/RMII	Two RGMII/RMII with MDIO at 1.8 V or 2.5 V
USB	Four USB 3.1 Gen 2; One shared with DisplayPort; Two USB 2.0
Functional safety	20 SM-GPIOs One SPI – master, One SPI – slave, Two I^2C – master 2-lane UART – master, Four clock monitors 44 voltage monitors pins Three on-board thermal monitors
Miscellaneous SPI I^2C UART GPIO	32 QUP SE (GPIO + SSC) Master and slave master Master Host 228 GPIOs
PMIC	32 GPIOs Seven AMUX

* The additional LS- I^2S interfaces (muxed with PCM/TDM pins) are configured from the three dedicated HS- I^2S interfaces.

3 Auto validation platform

The validation platform for SA8295P/QAM8295P is designed to enable enhanced test and debug of the chipset/module. The platform consists of the main board, SoC/SiP daughtercard, and a combination of multiple CCAs including, but not limited to, VIP, display, Ethernet, radio, camera, UFS, connectivity, sensor, and various test cards and connectors.

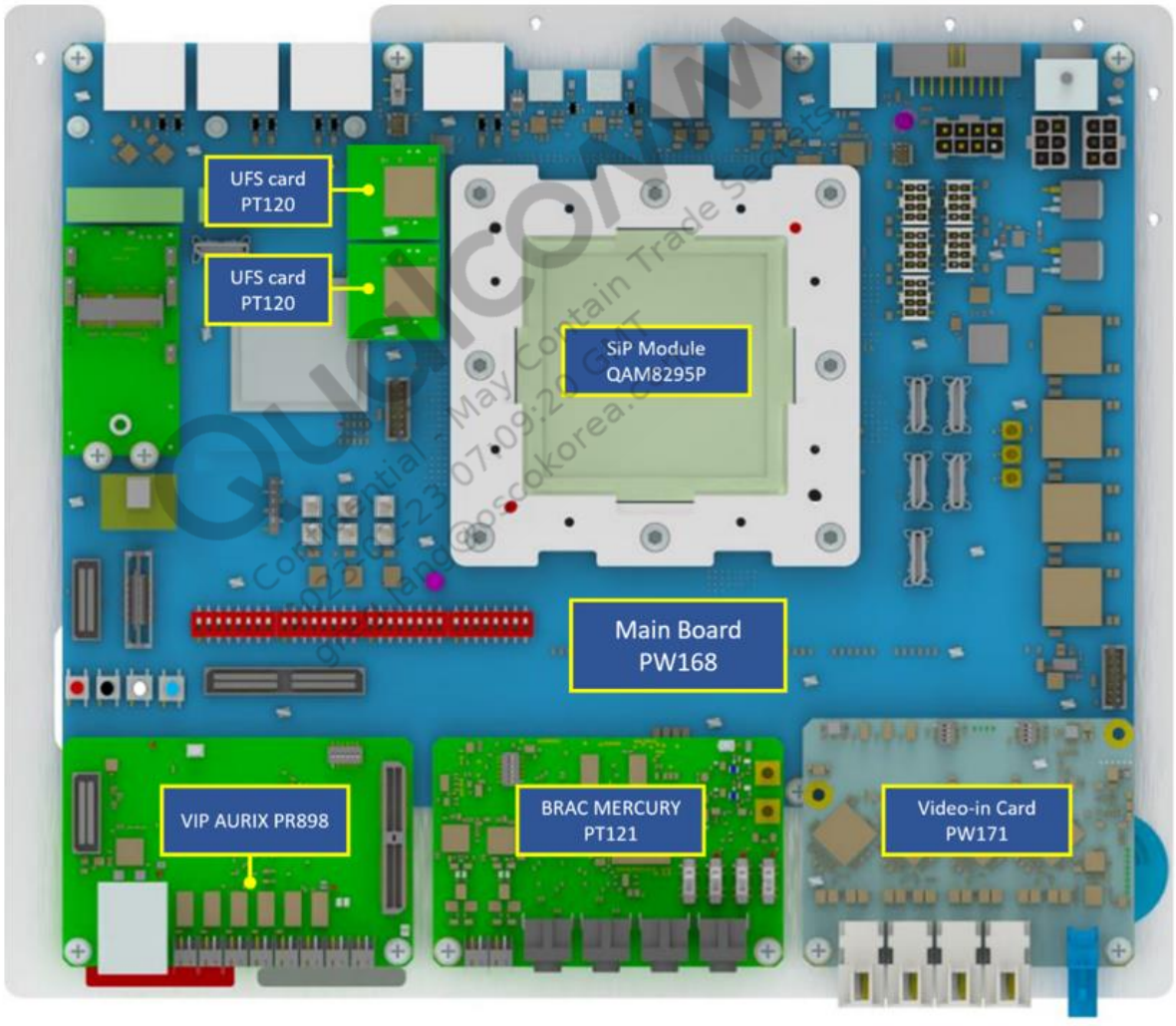


Figure 3-1 SA8295P/QAM8295P validation platform

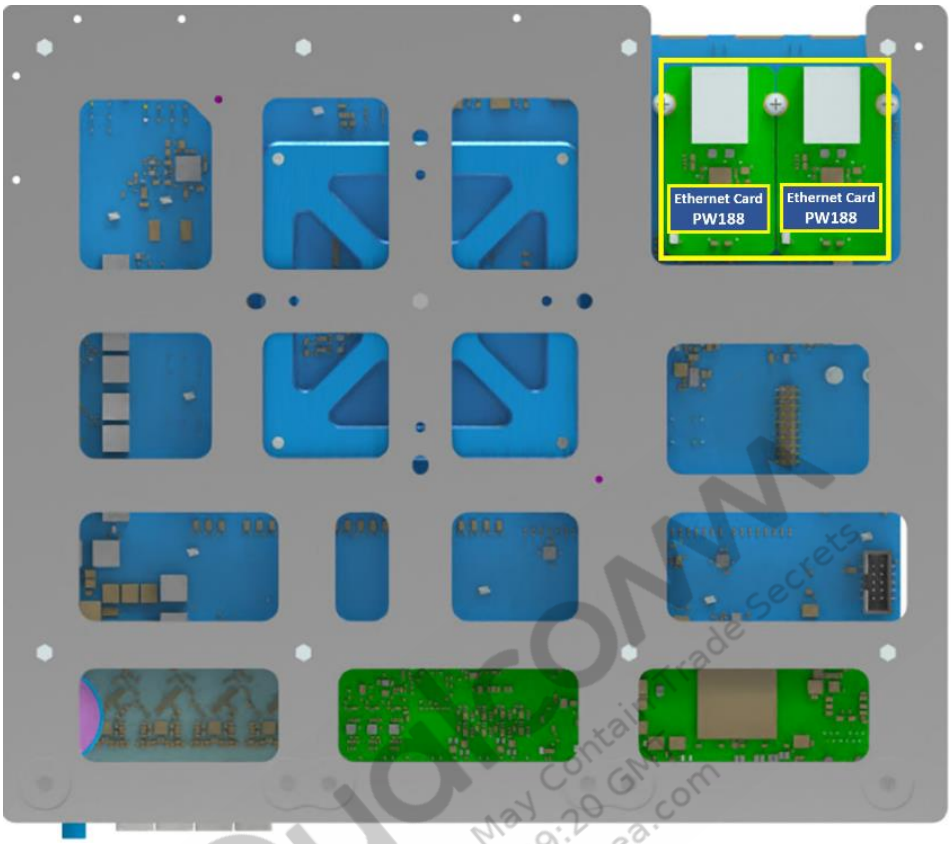


Figure 3-2 SA8295P/QAM8295P validation platform bottom side

3.1 Board summary of auto validation platform

Auto validation platform (ADP) assembly consists of a list of boards/subassemblies as listed in Table 3-1. The location of the boards/subassemblies is shown in Figure 3-1 and Figure 3-2.

Table 3-1 Board summary

Description	Board number
Main board	PW168
Vehicle Interface Processor (VIP) card	PR898
Camera card	PW171
Radio-Audio card	PT121
Ethernet card	PW188
UFS card	PT120

NOTE: *See Design Package, QAM8295P Automotive Development Platform Design Files* (DP25-PU692-40) for more details.

3.2 Ports and interfaces

The ADP STAR platform has various ports and interfaces that can connect to other functional blocks such as VIP, camera, audio and standard interfaces like Ethernet and PCIe. The ADP STAR daughtercards, ports, and interfaces are as shown in Figure 3-3, Figure 3-4, Figure 3-5, and connector details are provided in Table 3-2.

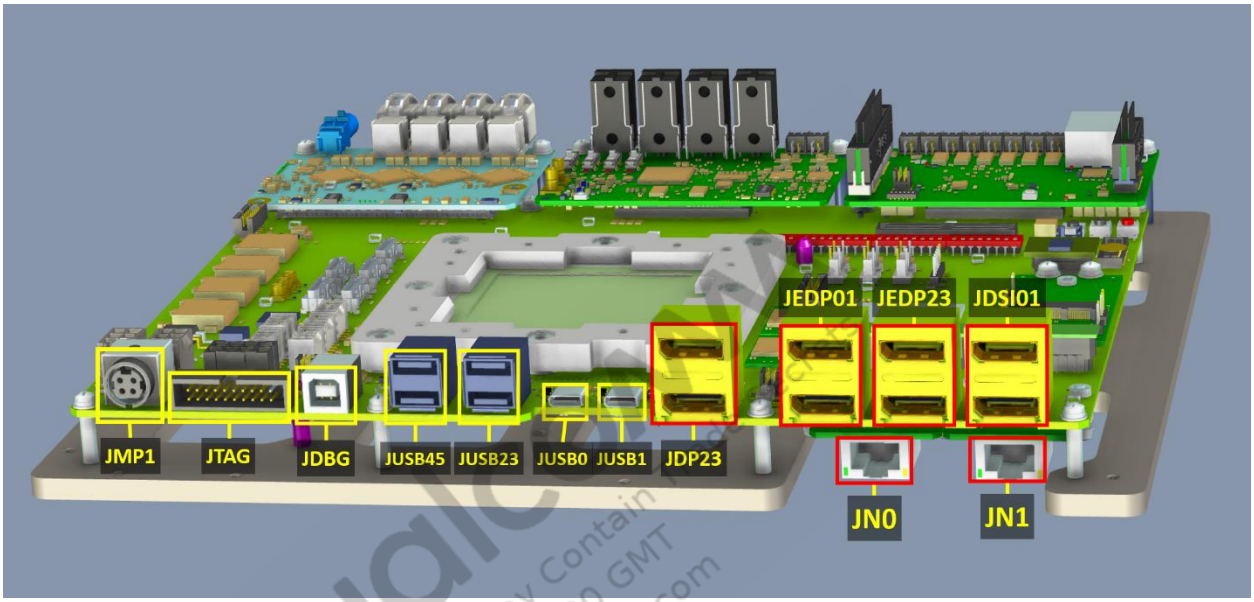


Figure 3-3 ADP STAR frontside connectors

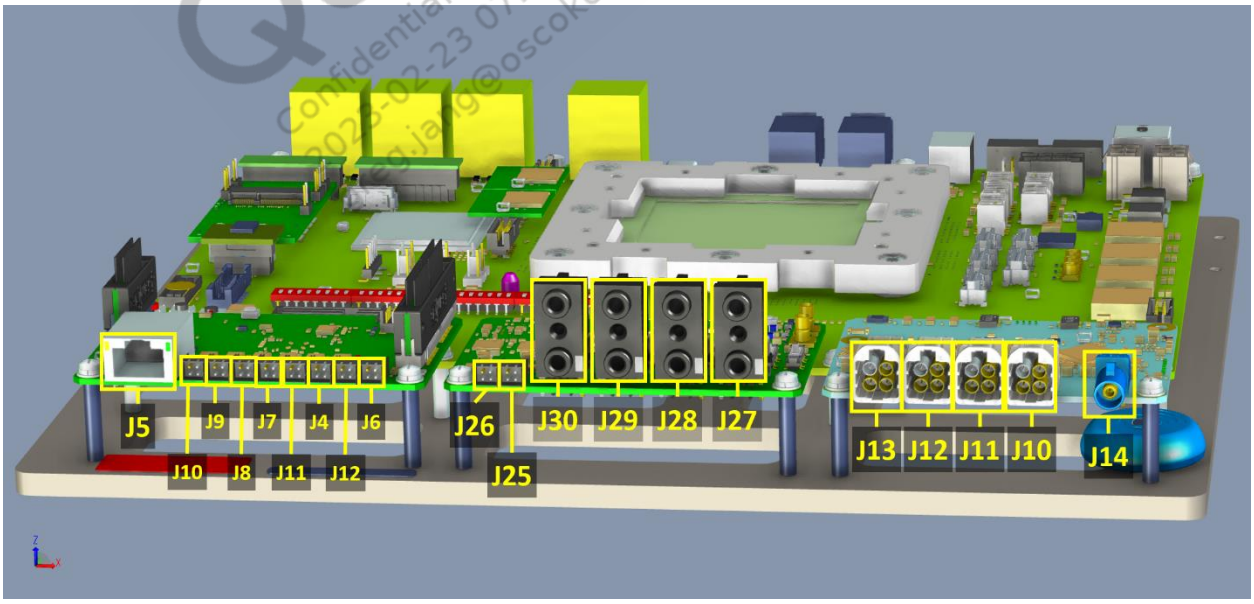


Figure 3-4 ADP STAR backside connectors

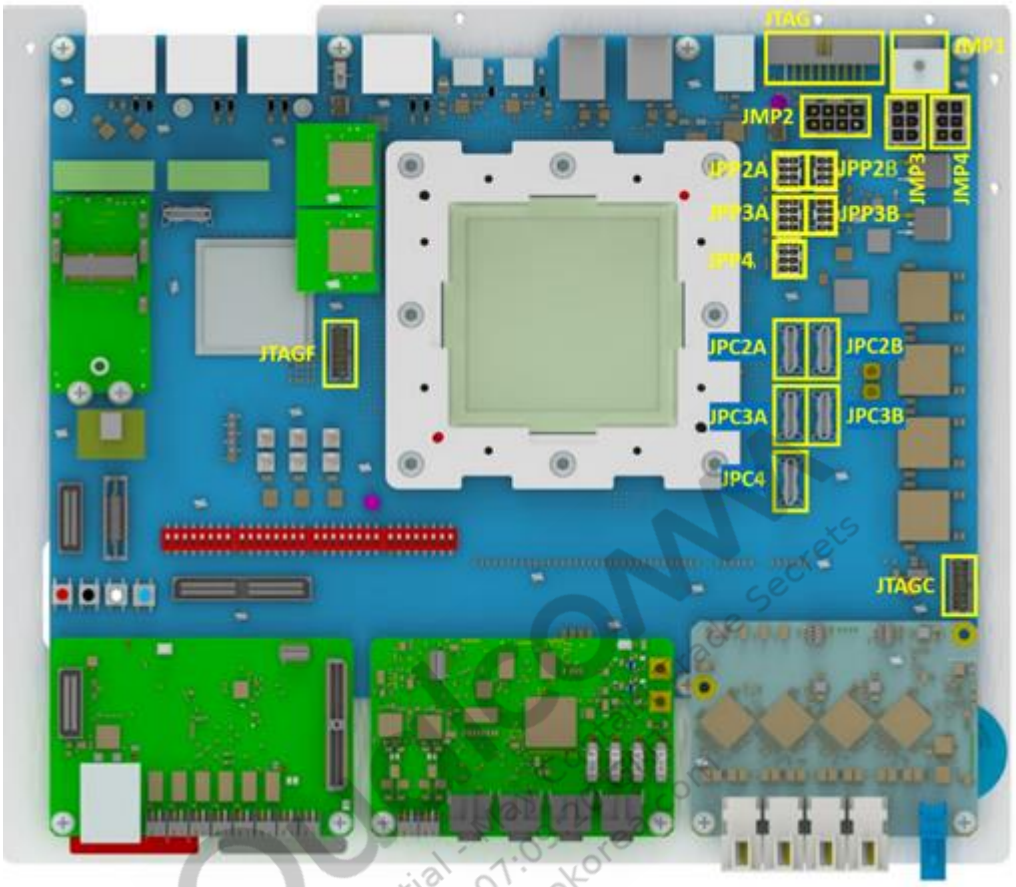


Figure 3-5 ADP STAR key ports and interfaces

Table 3-2 Power and JTAG connector details in ADP STAR platform

Connectors	Function
JDBG	Type-B USB connector used to interface onboard PSoC, SPI interface to FPGA, SoC APPSS UART, SoC SMSS UART, and VIP UART.
JTAG	QAM8295P JTAG connector for a standard Arm JTAG Lauterbach debug module.
JTAGF	JTAGF header to program the SPI configuration FLASH for the ARTIX-7 XC7A200T-2FFG1156I
JTAGC	JTAGC header to program the SPI configuration FLASH for the ARTIX-7 XC7S6-1CPGA196I on the gmsl2 Video in Card, PW171.
JMP1	Main power connector for 12 V power input
JMP2	Reserved
JMP3	Mini-Fit Jr. connector to be used when a bench top power supply or GST280A supply is needed for 12 V main. Either JMP3 or JMP4 or both can be used in this configuration.
JMP4	Mini-Fit Jr. connector to be used when a bench top power supply or GST280A supply is needed for 12 V main. Either JMP3 or JMP4 or both can be used in this configuration.

NOTE: For interface connectors, see individual daughter card sections.

3.3 Validation platform architecture

The ADP STAR board has main board implementation with SA8295P SoC and QAM8295P module. The following subsection provides the architecture details of the implementation.

3.3.1 ADP STAR board architecture with QAM8295P module

The architectural block diagram of ADP STAR implementation with QAM8295P module is as shown in Figure 3-6. The platform consists of the main board with the QAM8295P soldered and interfacing connectors for other module cards that cover all the functional requirements.

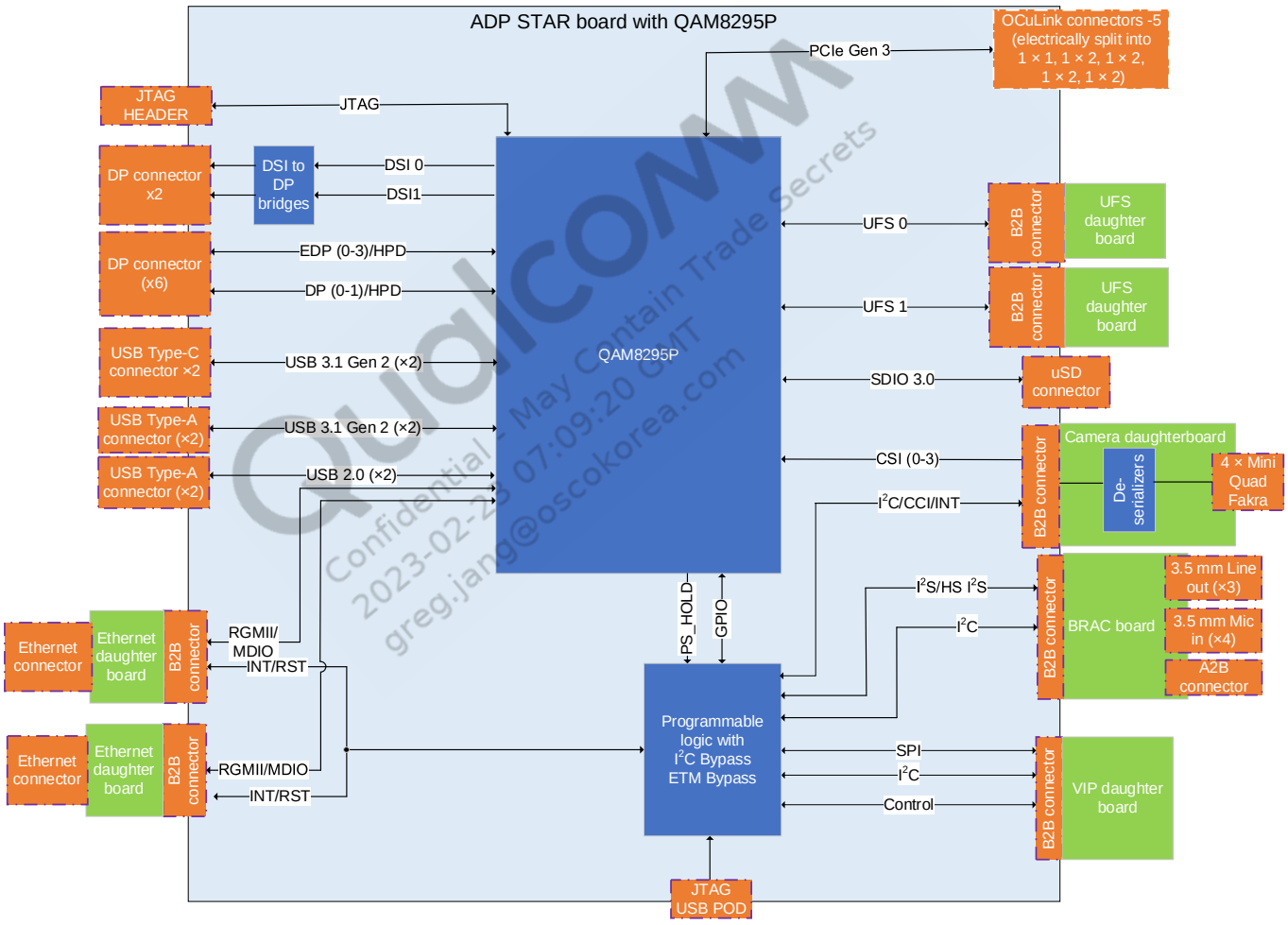


Figure 3-6 ADP STAR board architecture with QAM8295P

4 Main board (PW168)

4.1 Main board architecture

The ADP STAR main board (PW168) uses the QAM8295P module and its implementation architecture is as shown in Figure 3-6. The PW168 consists of a user interface that includes buttons, switches, and LEDs. There are interface connectors that connect to system interfaces or other cards to implement supplementary functions. The PW168 includes an FPGA to provide an interface to a PC, allowing control of various platform interfaces. The FPGA also provides an interface to the SoC, to control all GPIO related interfaces.

The ADP STAR main board has provision to connect the following peripheral cards:

- Vehicle interface processor (VIP) card
- Broadcast radio and audio card (BRAC)
- Camera/video-in card
- Ethernet card
- UFS card

The following subsections provide details of the main board (PW168) implementation including the user interface, peripheral interface, FPGA, and power supply section details.

4.2 System power supplies

The ADP STAR main board is powered from a 12 V power source. The ADP STAR board input voltage range is 6 V to 20 V DC. It is recommended to use a 12 V, 5 A power source. The required power for QAM8295P and other onboard peripherals is generated by the onboard power supply as shown in Figure 4-2.

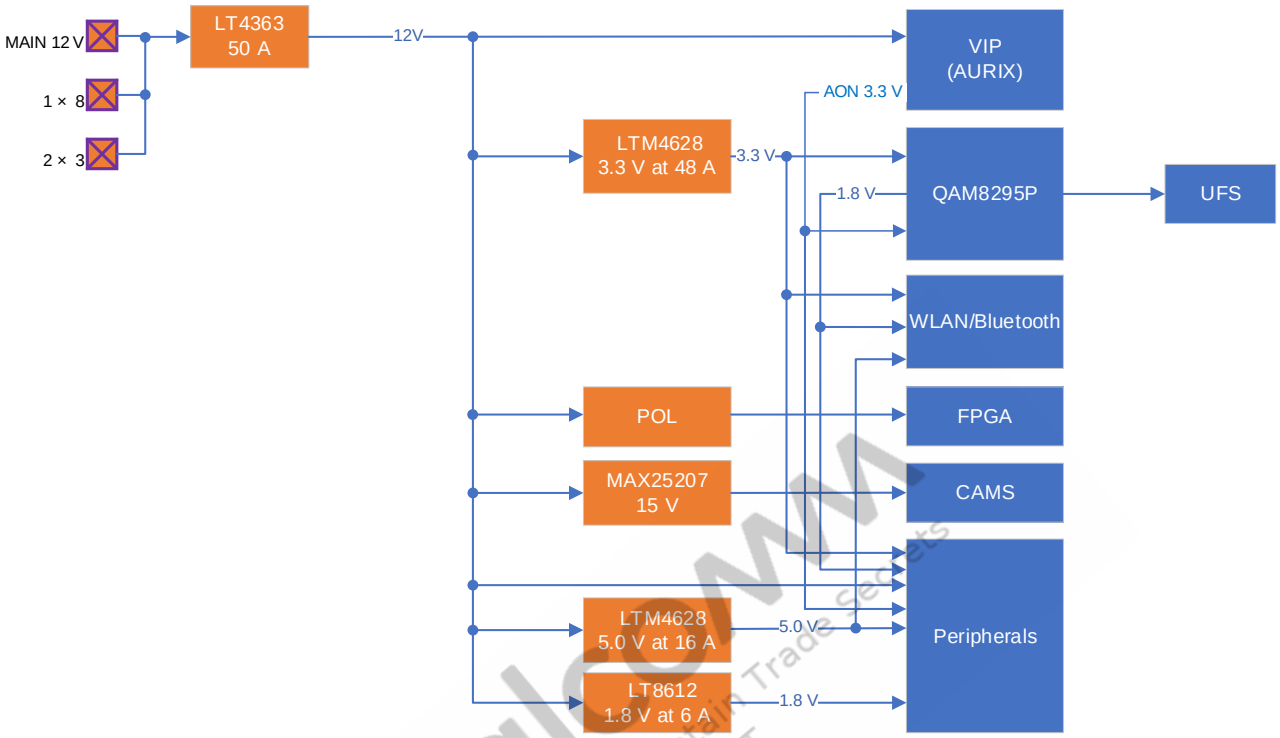


Figure 4-1 ADP STAR power tree

4.3 User interfaces

ADP STAR user interface consists of DIP switches, buttons, and LED indicators as shown in Figure 4-2. The following sections provide details of the user interfaces.

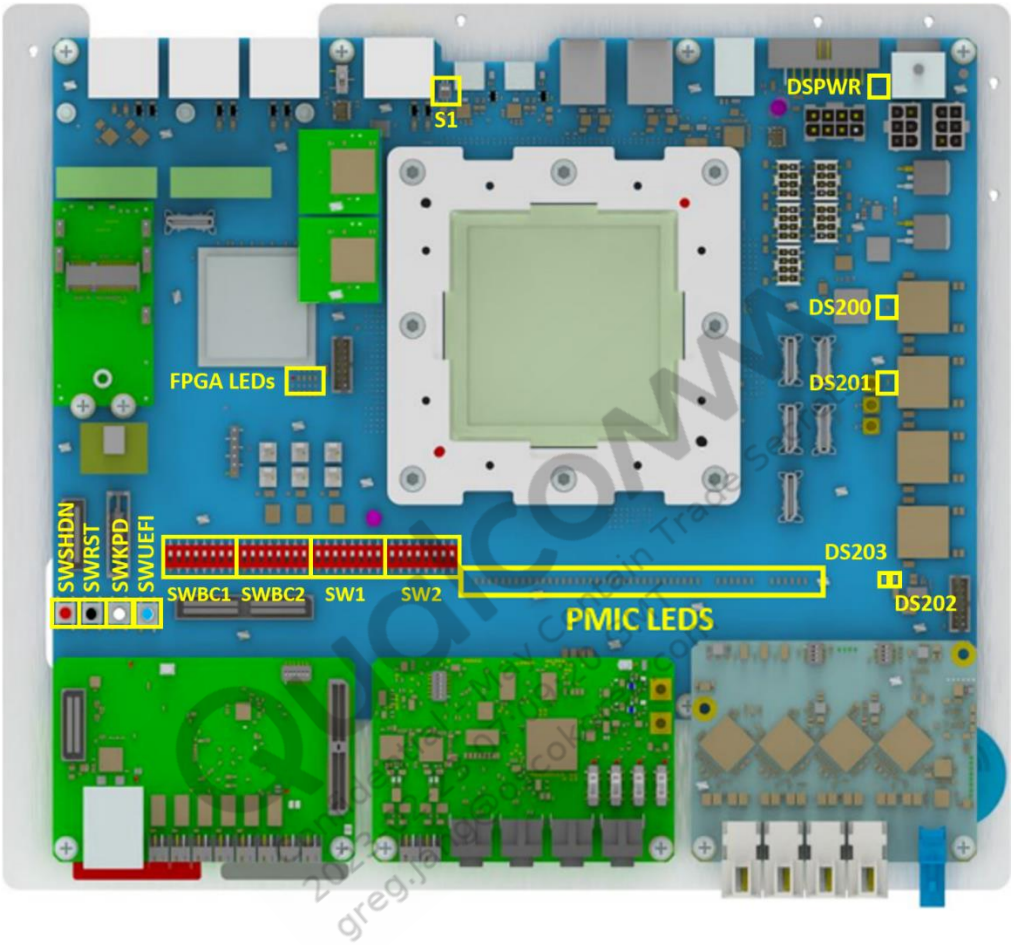


Figure 4-2 ADP STAR buttons, switches and LEDs location

4.3.1 DIP switches

The ADP STAR DIP switches as shown in Figure 4-2, allow the user to set the QAM8295P boot configuration. Details of the boot configuration switches are listed in Table 4-1.

Table 4-1 Boot configuration switches

Ref	Pos	Function	State	Logic	Usage					
SWBC1	1-5	Reserved								
	6	FORCE USB BOOT (EDL)	OFF	LOW	ON - HIGH = Force EDL					
	7, 8	MODE [1:0]	OFF	LOW	Function	Mode				
					00	TRACE32				
					11	Boundary scan mode				
					10, 01	Reserved				
SWBC2	1	WATCH DOG DISABLE	ON	HIGH	HIGH = Disable Watchdog					
					LOW = Enable Watchdog					
	2, 3, 4, 5	Fastboot SEL [3:0]	OFF	LOW		3	2	1	0	
					UFS HS G1→ USB	0	0	0	0	
	6, 7, 8	Reserved								

Table 4-2 Boot configuration switches (SW1 and SW2)

Ref	Pos	Function	State	Logic	Usage
SW1	1	CAM MODE SEL 0	OFF	LOW	See Chapter 8 for details on these control pins
	2	CAM MODE SEL 1	OFF	LOW	
	3	CAM MODE SEL 2	OFF	LOW	
	4	CAM MODE SEL 3	OFF	LOW	
	5	VIP SoC BC EN	OFF	LOW	ON - HIGH = Enable VIP control of Boot Config
					OFF - LOW = Disable VIP control of Boot Config
	6	RESIN BYPASS CTRL	OFF	LOW	
	7	EUD EN	OFF	LOW	
	8	SMSS I^{2}C MASTER SEL	OFF	LOW	
SW2	1	ETM A SEL	OFF	LOW	ON - HIGH = ETM Bus A enabled
					OFF - LOW = ETM Bus A not enabled
	2	ETM B SEL	OFF	LOW	OFF - HIGH = ETM Bus B enabled
					OFF - LOW = ETM Bus B not enabled
	3	SoC JTAG DET OVERIDE	OFF	LOW	LOW = PS_HOLD not forced with JTAG connected
					HIGH = PS_HOLD is forced with JTAG connected
	4	SW2 POS4 SPARE	OFF	LOW	
	5	SW2 POS5 SPARE	OFF	LOW	
	6	SW2 POS6 SPARE	OFF	LOW	
	7	PGA MODE SEL			Reserved
	8	SiP PROTO RPOD SEL			Reserved

For all the DIP switches except switch 2.7 and switch 2.8

ON is logic HIGH; OFF is logic LOW

4.3.2 USB ports 0 and 1 power control

Table 4-3 provides the USB power control options for client and host mode operations.

Table 4-3 USB port power control

Ref	Pos	USB port	State	Function
S1	1	1	ON	USB Client Mode - no power on connector
			OFF	USB Host Mode - 5V Power on connector WARNING: No current limiting in this mode. Use care not to damage your platform.
	2	0	ON	USB Client Mode - no power on connector
			OFF	USB Host Mode - 5V Power on connector WARNING: No current limiting in this mode. Use care not to damage your platform.

4.4 Main board buttons

The ADP STAR main board button location is shown in Figure 4-2. The functions of the main board buttons are listed in Table 4-4.

Table 4-4 Main board button functions

Ref	Color	Function
SWSHDN	RED	Press and hold to disable power to the entire platform. This is the easiest way to power cycle the entire platform. WARNING: This will turn off all the power supplies, including the power supply at VIP.
SWRST	BLACK	This button is mapped to PMIC RESIN
SWKPD	WHITE	This button will initiate a platform PON if the platform is off. After a successful platform PON, this is mapped to PMIC KPDPWR.
SWUEFI	BLUE	Force the SoC to boot into UEFI console.

4.5 LED indicators

The ADP STAR main board has indications for main input power status, PMIC power rail status, and FPGA debug status with details in the following sub-sections.

4.5.1 Main power LEDs

The Main power LEDs indicate the status of the input power and the power rails on the ADP STAR board. The LED reference and corresponding indication functions are as shown in Figure 4-2 and are listed in Table 4-4.

Table 4-5 Main power LED functions

Ref	Color	Indication
DSPWR	BLUE	Main 12 V power in
DS200	GREEN	VREG 5.0 V power good
DS201	GREEN	VREG 3.3 V power good
DS202	GREEN	VREG 1.8 V power good
DS203	GREEN	VREG CAM power good

4.5.2 PMIC LEDs

The location of the PMIC LEDs is outlined in Figure 4-2. Figure 4-3 is a zoomed-in version with details of power rail indication per LED. The LED ON indicates that power rail is ON. All the PMIC LEDs are GREEN.

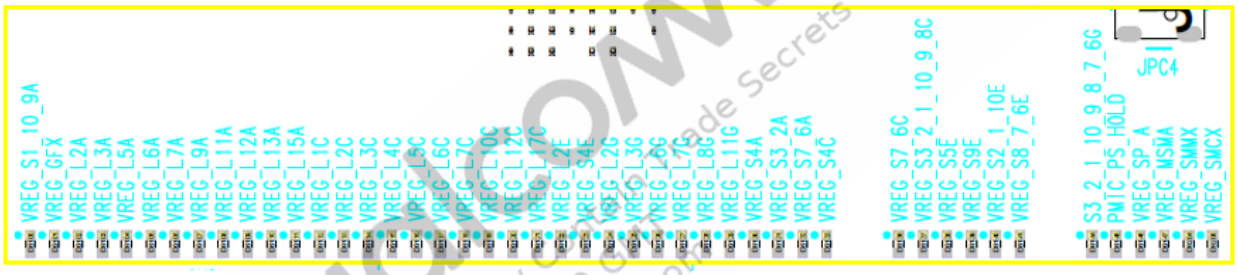


Figure 4-3 PMIC LEDs location and function

4.5.3 FPGA LEDs

The location of FPGA LEDs is outlined in Figure 4-2. Figure 4-4 is a zoomed-in version with location details of the LEDs. The FPGA Debug LEDs (0-6) are used for status and debug of the platform as listed in Table 4-6.

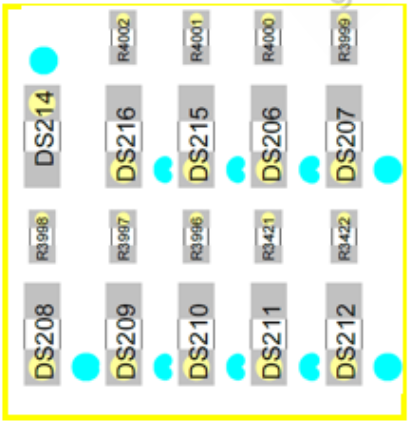


Figure 4-4 FPGA LED location

Table 4-6 FPGA LED functions

REF	Color	Function
DS214	RED	Indicates that the FPGA is in a reset state.
DS216	GREEN	FPGA debug LED (0). (Default = S4A_VALID_1P8)
DS215	GREEN	FPGA debug LED (1). (Default = PMIC_RESIN_S4A_1P8_ODO_N)
DS206	GREEN	FPGA debug LED (2). (Default = PMIC_FAULT_VIP_3P3)
DS207	GREEN	FPGA debug LED (3). (Default = SOC_RESIN_S4A_1P8_N)
DS208	GREEN	FPGA debug LED(4). (Default = SOC_RESOUT_S4A_1P8_N)
DS209	GREEN	FPGA debug LED(5). (Default = PMIC_PS_HOLD_S4A_1P8)
DS210	GREEN	FPGA debug LED(6). (Default = AOSS_SLP_IND_S4A_1P8)
DS211	GREEN	SMSS_LED(1)
DS212	GREEN	SMSS_LED(2)

4.6 Display overview

SA8295P has two independent Display Processor Unit (DPUs) integrated, which provides two dedicated DisplayPorts and four dedicated eDPs. Each DisplayPort/eDP interface has a dedicated GPIO assigned for Hot Plug Detection (HPD) as shown in Figure 4-5.

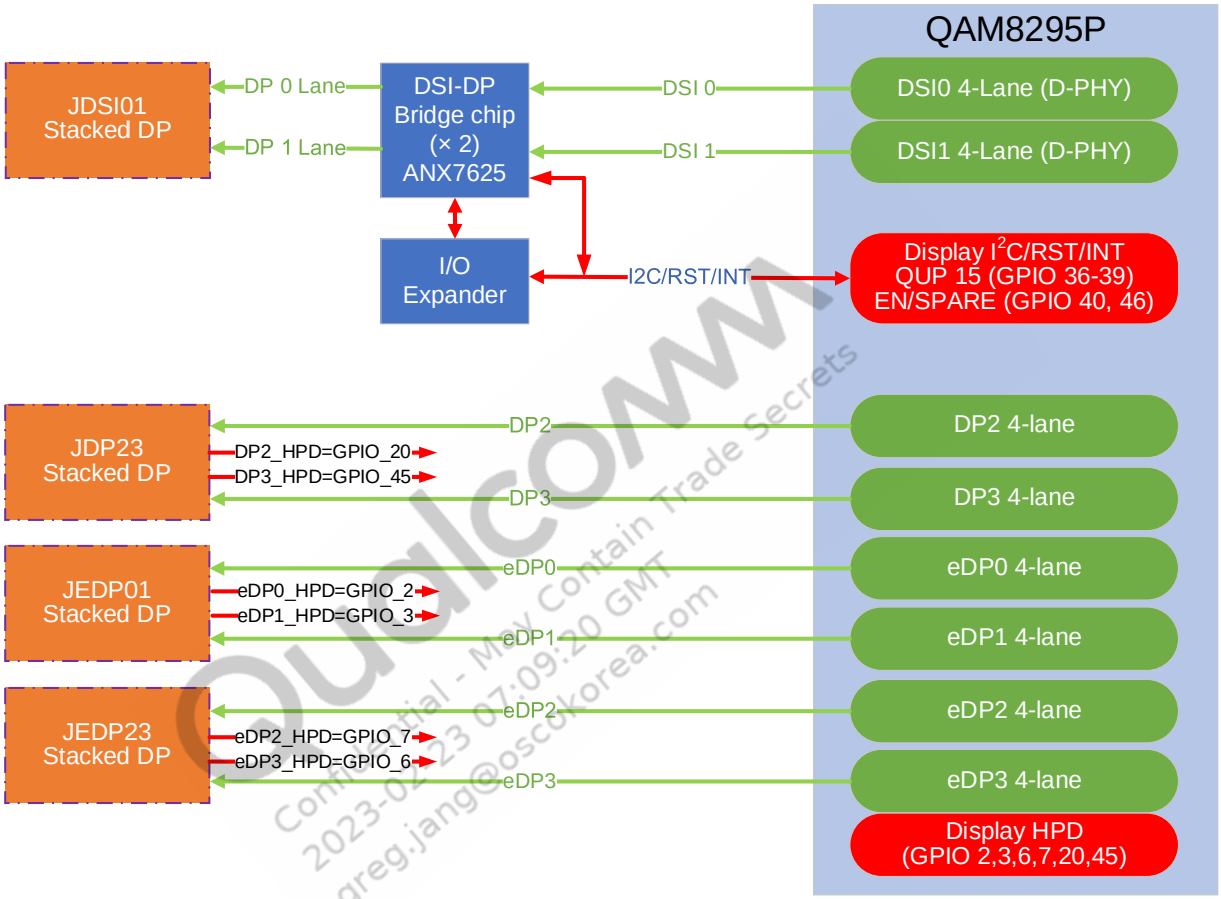


Figure 4-5 DisplayPort interface

Table 4-7 Display interface connector details

Connectors	Function
JDP23	Stacked DisplayPort 1.4 receptacle. Top connector interfaces with QAM8295P DP2 4-lane interface and the bottom interfaces to QAM8295P DP3 4-lane interface.
JEDP01	Stacked DisplayPort 1.4 receptacle. Top connector interfaces with QAM8295P eDP0 4-lane interface and the bottom interfaces to QAM8295P eDP1 4-lane interface.
JEDP23	Stacked DisplayPort 1.4 receptacle. Top connector interfaces with QAM8295P eDP2 4-lane interface and the bottom interfaces to QAM8295P eDP3 4-lane interface.
JDSI01	Stacked DisplayPort 1.4 receptacle. Top and bottom connector interfaces with DSI0 2-lane and DSI1 2-lane interface respectively of QAM8295P through a DSI to DisplayPort bridge IC (ANX7625).

4.7 USB overview

The USB interface of the ADP STAR board is connected to the SA8295P on the QAM8295P module. The SA8295P has six USB interfaces as shown in Figure 4-6 with the following features:

- USB 0/USB 2/USB 3 – dedicated USB 3.1 Gen 2 SS + HS
- USB 0 interface is also used for emergency download mode
- USB 1 – dedicated USB 2.0 + shared SuperSpeed pins with DisplayPort
- USB 4/USB 5 – dedicated USB 2.0 only
- USB 2/USB 3/USB 4/USB 5 can only support host mode

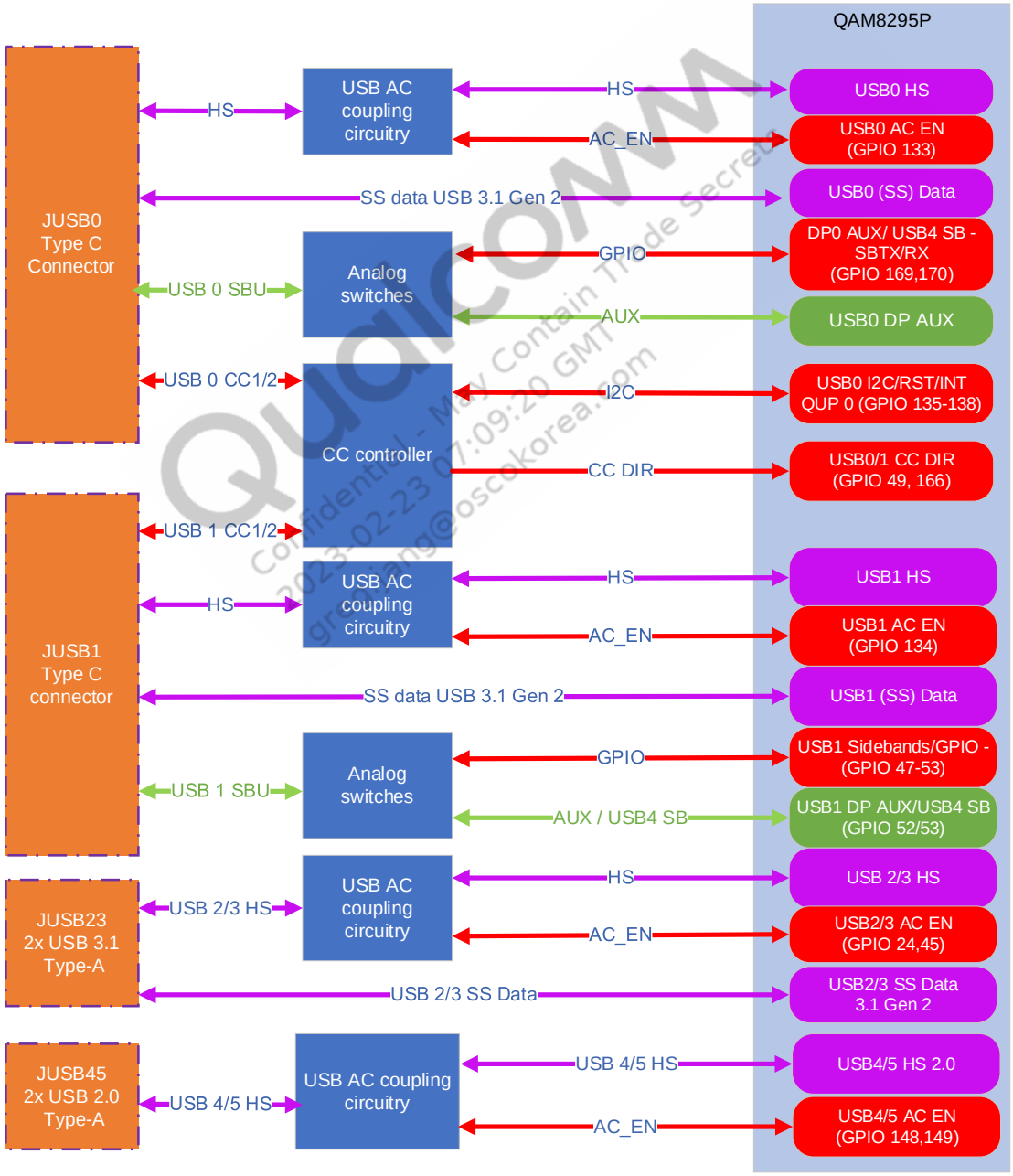


Figure 4-6 USB interfaces

There is an USB based debug interface on ADP STAR that connects the UART and JTAG debug port of QAM8295P through an onboard USB hub as shown in Figure 4-7. The connector details of all the USB interfaces are listed in Table 4-8.

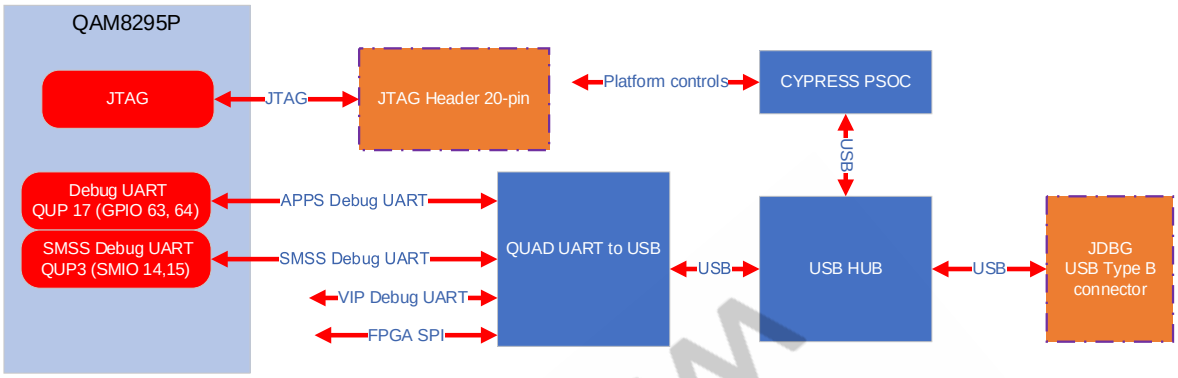


Figure 4-7 USB debug port

Table 4-8 USB and debug connectors

Connectors	Function
JDBG	Type-B USB connector used to interface onboard PSoC, SPI interface to FPGA, SoC APPSS UART, SoC SMSS UART, and VIP UART.
JUSB45	Stacked USB 3.1 Gen 2 Type-A receptacle. Top connector interfaces to USB 5 of QAM8295P and bottom connection interfaces to USB 4 of QAM8295P. Both support only HS connections.
JUSB23	Stacked USB 3.1 Gen 2 Type-A receptacle. Top connector interfaces to USB 3 of QAM8295P and bottom connection interfaces to USB 2 Bus of QAM8295P. Both support HS and SS USB connections.
JUSB0	USB 3.1 Gen 2 Type-C receptacle that interfaces to USB 0 HS/SS interface of QAM8295P
JUSB1	USB 3.1 Gen 2 Type-C receptacle that interfaces to USB 1 HS/SS interface of QAM8295P

4.8 PCIe (OCuLink) overview

The PCIe interface details on the ADP STAR is shown in Figure 4-8. The OCuLink cable can be used for connecting the PCIe interface to PCIe daughter boards.

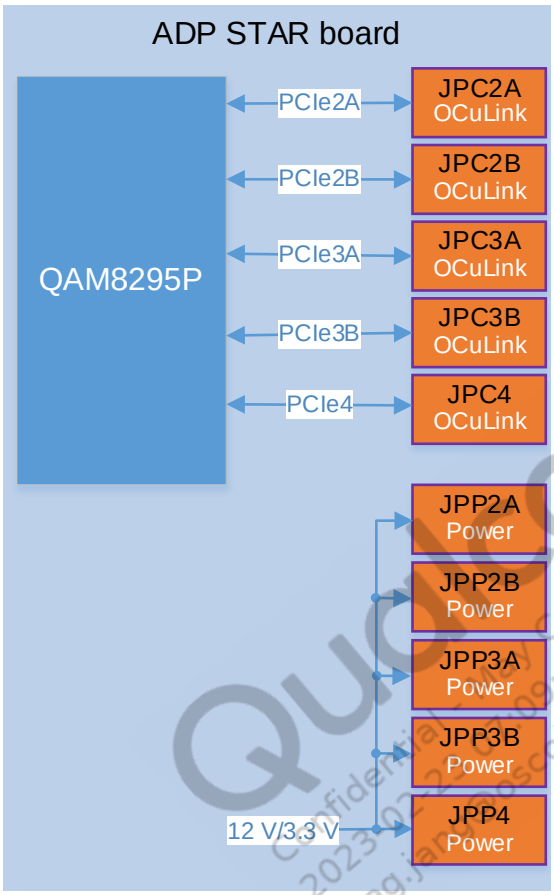


Figure 4-8 ADP STAR PCIe interface

Table 4-9 PCIe interface connectors

Connectors	Function
JPC2A	PCIe Gen4 Vertical launch connector. Two-lane PCIe from QAM8295P PCIe2A interface.
JPC2B	PCIe Gen4 Vertical launch connector. Two-lane PCIe from QAM8295P PCIe2B interface.
JPC3A	PCIe Gen4 Vertical launch connector. Two-lane PCIe from QAM8295P PCIe3A interface.
JPC3B	PCIe Gen4 Vertical launch connector. Two-lane PCIe from QAM8295P PCIe3B interface.
JPC4	PCIe Gen4 Vertical launch connector. One-lane PCIe from QAM8295P PCIe4 interface.
JPP2A	Power accessory header for JPC2A interface. Supplies 3.3 V and 12 V to PCIe device.
JPP2B	Power accessory header for JPC2B interface. Supplies 3.3 V and 12 V to PCIe device.
JPP3A	Power accessory header for JPC3A interface. Supplies 3.3 V and 12 V to PCIe device.
JPP3B	Power accessory header for JPC3B interface. Supplies 3.3 V and 12 V to PCIe device.
JPP4	Power accessory header for JPC4 interface. Supplies 3.3 V and 12 V to PCIe device.

4.9 FPGA

The QAM8295P ADP STAR board contains an FPGA that interfaces to both a PC and the QAM8295P via separate SPI interfaces. These SPI interfaces provide all the communications to the FPGA sub-blocks that connect to other interfaces internal to the ADP-STAR board, as indicated in Figure 4-9.

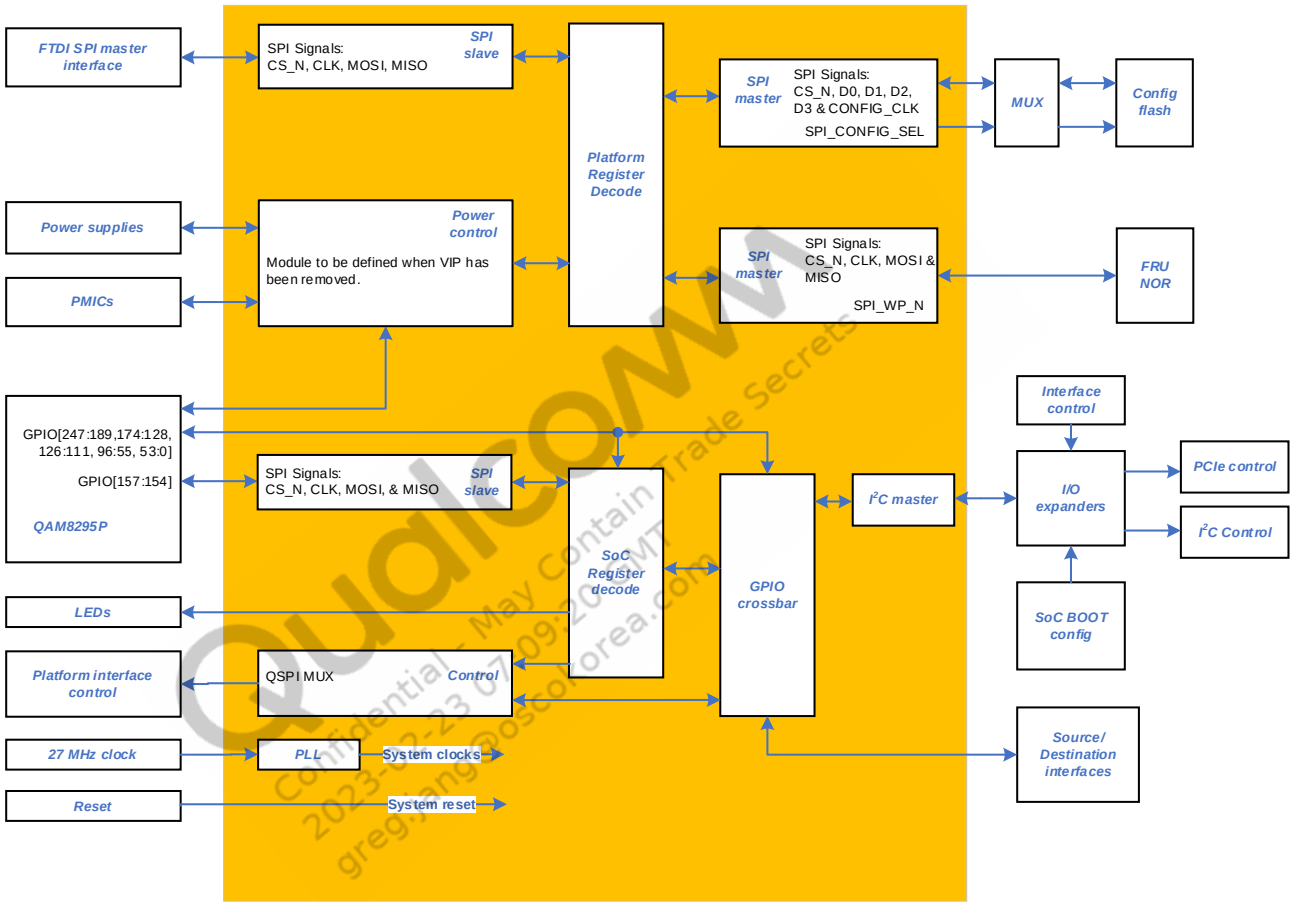


Figure 4-9 FPGA implementation on the QAM8295P ADP STAR board

5 VIP (AURIX) daughtercard (PR898)

5.1 VIP (AURIX) function overview

The primary Aurix TC399 provides supervisory and control signals for the QAM8295P automotive development platform. Most ASIL D processing is done on this device. Main power supplies, power sequences, reset trees, SoC power-up, cooling fan, and so on, are controlled by the VIP. The VIP communicates with the vehicle buses via CAN-FD and LIN, and with the SoC via SPI and UART. The secondary Aurix TC397 provides extra ASIL D MIPS for certain use cases and is not required for basic system operation.

5.1.1 Interface

- External connector for CAN, LIN, power input: molex sTAK50H 200502-0321:

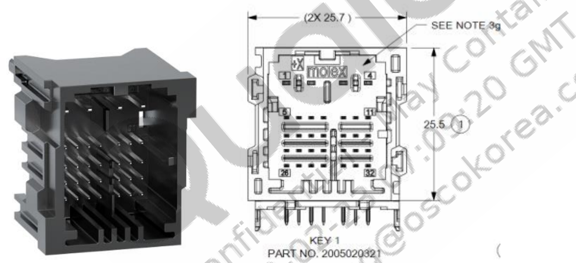


Figure 5-1 molex sTAK50H 200502-0321

- Pinout for molex sTAK50H 200502-0321

Table 5-1 Pinout for molex sTAK50H 200502-0321

1	VBATT_IN	2	VBATT_IN	3	GND	4	GND						
5	CAN1_P	6	CAN1_M	7	CAN2_P	8	CAN2_M	9	MCU_OUT1_3P3	10	SW_12V	11	SOC_OUT3_3P3
12	CAN3_P	13	CAN3_M	14	CAN4_P	15	CAN4_M	16	MCU_OUT2_3P3	17	NC	18	SOC_OUT2_3P3
19	CAN5_P	20	CAN5_M	21	CAN6_P	22	CAN6_M	23	MCU_OUT3_3P3	24	NC	25	SOC_OUT1_3P3
26	LIN0	27	GND	28	LIN1	29	GND	30	MCU_OUT4_3P3	31	NC	32	GND

- Breakout board needed to separate out interfaces to individual connectors

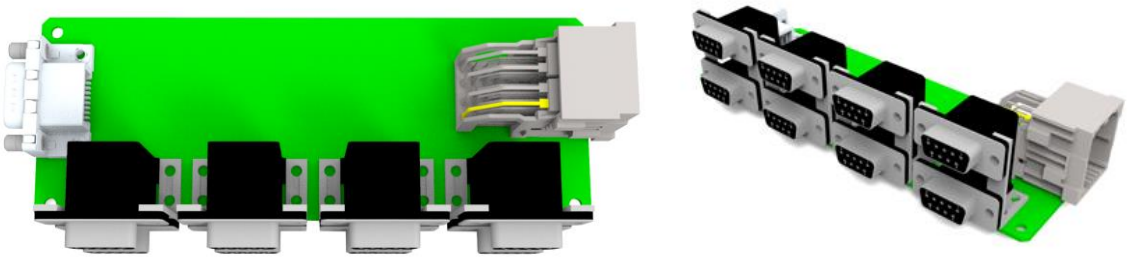


Figure 5-2 CAN LIN breakout board mechanical (preliminary)

- For debug connector pinouts, see Infineon documentation:

Infineon-ApplicationKitManual_TC3X7-UM-v02_00-EN.pdf

Table 5-2 VIP (CAN, LIN, and Ethernet interface connectors)

Connectors	Function
J10	CAN Bus(6)
J9	CAN Bus(5)
J8	CAN Bus(4)
J7	CAN Bus(3)
J11	CAN Bus(2)
J4	CAN Bus(1)
J12	LIN Bus(2)
J6	LIN Bus(1)
J5	VIP Aurix Gigabit Ethernet Connector

5.1.2 VIP (AURIX) block diagram

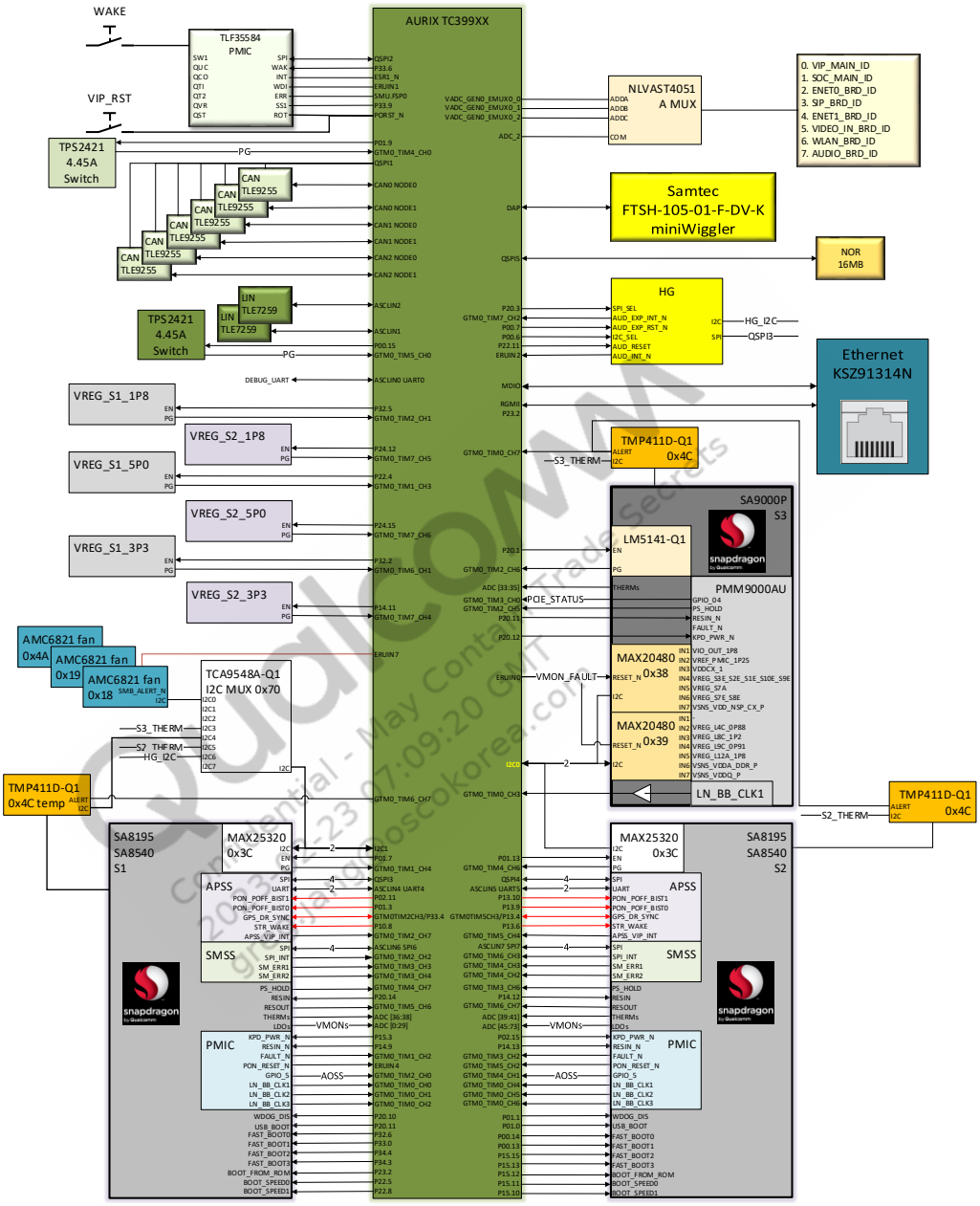


Figure 5-3 VIP (AURIX) block diagram

NOTE: The PM_FAULT_N signal is connected to the VIP for QTI debug purposes as shown in the figure. Customer is not required to monitor the PM_FAULT_n as part of safety, and should not connect to it.

6 Ethernet daughtercard (PW188)

6.1 Ethernet feature overview

- Supports 10/100/1000 Base-T
- Supports both RGMII and RMII buses to allow the testing of the Ethernet MAC inside of the SoC
- Feature LEDs on reset signals and related power rails

6.2 Mechanical

External connector for Ethernet Amphenol: RJMG2012119A0NR

Figure 6-1 RJ45 Ethernet connector

6.3 Ethernet card (PW188) block diagram

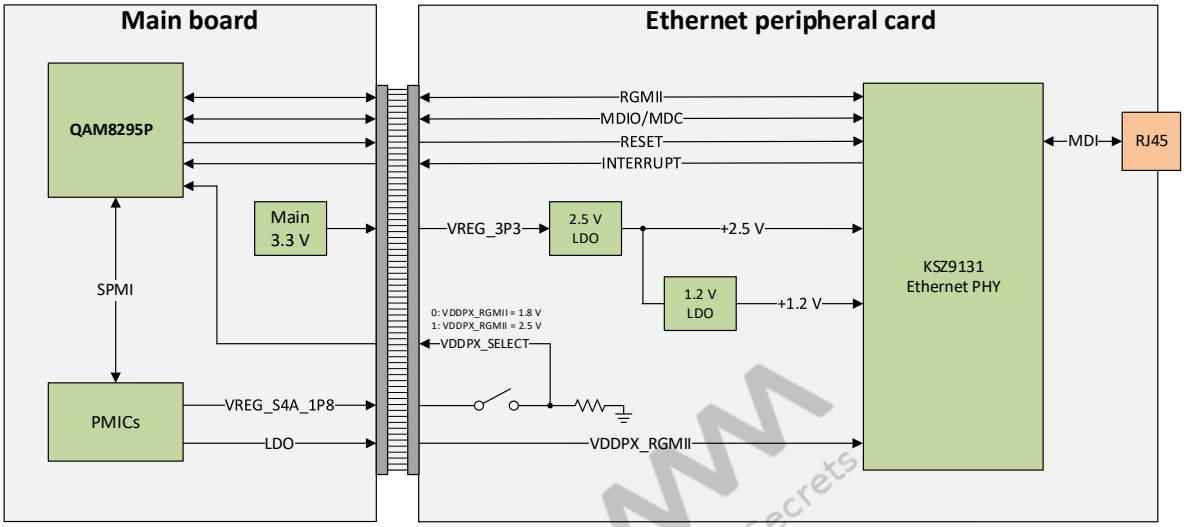


Figure 6-2 Ethernet card (PW188) block diagram

Table 6-1 Ethernet interface connectors

Connectors	Function
JN0	Ethernet connector interfaces with the RGMII(0) Bus on the QAM8295P
JN1	Ethernet connector interfaces with the RGMII(1) Bus on the QAM8295P

7 BRAC daughtercard (PT121)

7.1 BRAC feature overview

- NXP Mercury (SAF4000) Car DSP chipset and digital input audio amplifier that supports up to 6 Class-D headphone amplifiers, FM/AM input, and S/PDIF input/output
- Four I^2S buses are used to interface with NXP Mercury (SAF4000) Car DSP chipset for broadcast radio and audio features

7.2 BRAC design card details

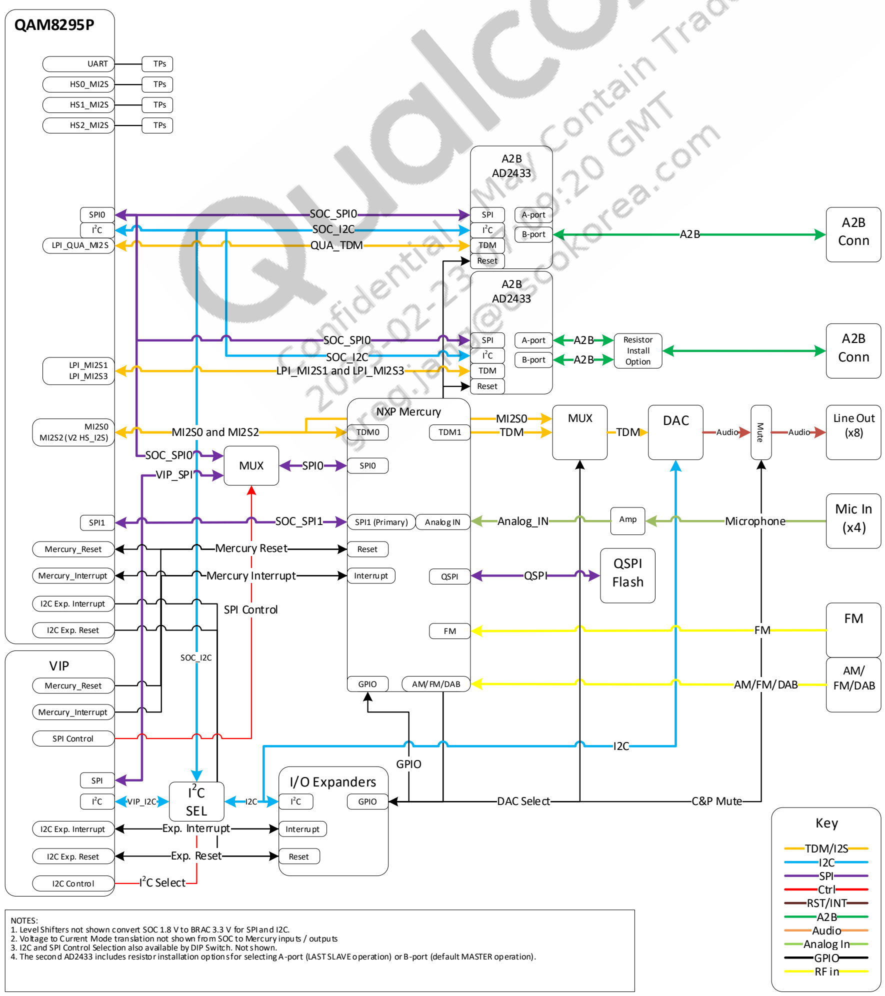


Figure 7-1 BRAC (PT121) block diagram

Table 7-1 BRAC interface connectors

Connectors	Function
J26	4-pin connector supports the interface to the A2B(2) Bus.
J25	4-pin connector supports the interface to the A2B(1) Bus.
J30	Dual stacked 3.5 mm jack supports the AudioOut(3) on the upper port and the AudioOut(4) on the lower port.
J29	Dual stacked 3.5 mm jack supports the AudioOut(1) on the upper port and the AudioOut(2) on the lower port.
J28	Dual stacked 3.5 mm jack supports the MIC(3) input on the upper port and MIC(4) input on the lower port.
J27	Dual stacked 3.5 mm jack supports the MIC(1) input on the upper port and MIC(2) input on the lower port.

8 Camera daughtercard (PW171)

8.1 GMSL camera card feature overview

GMSL Camera card (features four quad FAKRA mini coaxial connectors, that support 16 camera inputs routed to both QAM8540Ps and the FAKRA connector for loopback camera output.

- Key components: GMSL card (PW171)
- Four quad deserializer (MPN: MAX96712GTB/VY+(ES))
- One Xilinx FPGA Spartan-7 6 K cells 100 I/O (MPN: XC7S6-1CPGA196I)
- One serializer (Maxim MPN: MAX9295AGTJ/V+)
- Camera connector: 4 Rosenberger, MPN: AMS22D-40MZ5-Z

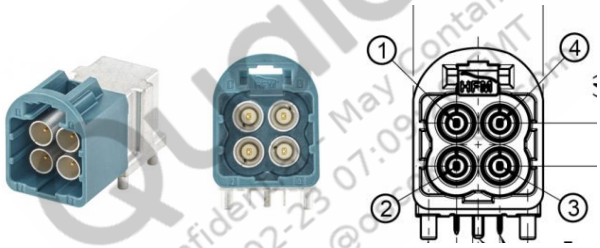


Figure 8-1 GMSL camera card connector

8.2 GMSL camera card (PW171) block diagram

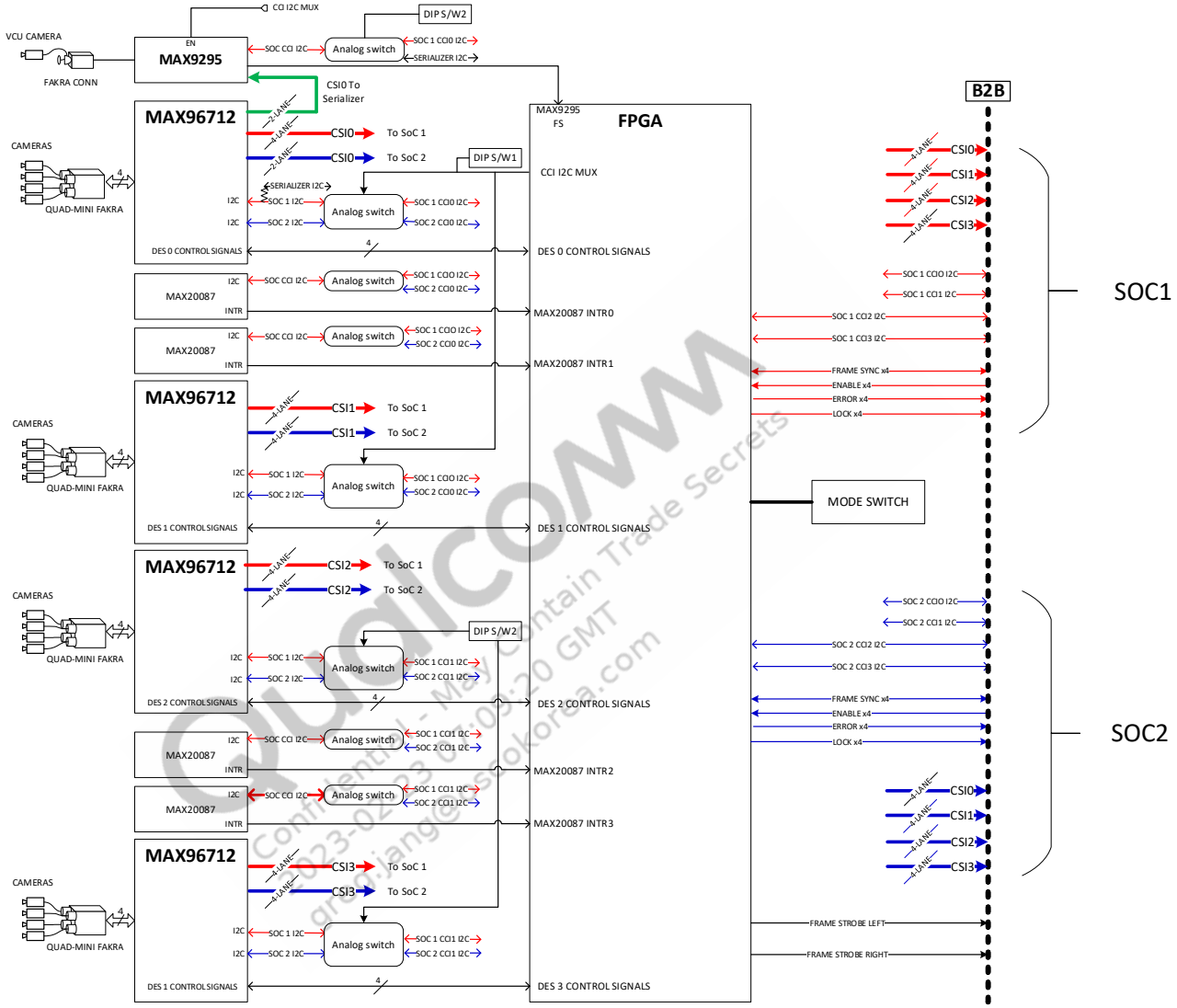


Figure 8-2 GMSL camera card (PW171) block diagram

Table 8-1 Camera interface connectors

Connectors	Function
J14	GMSL output loopback to J10–J13 inputs for loop back testing.
J13	Connects to CSI(3) interface of QAM8295P post the GMSL to CSI deserializer.
J12	Connects to CSI(2) interface of QAM8295P post the GMSL to CSI deserializer.
J11	Connects to CSI(1) interface of QAM8295P post the GMSL to CSI deserializer.
J10	Connects to CSI(0) interface of QAM8295P post the GMSL to CSI deserializer.

9 Flash memory daughtercard (PT120)

9.1 UFS card (PT120) overview

There is one 80-pin connector on the SoC daughter card for interfacing with a UFS 3.0 card.

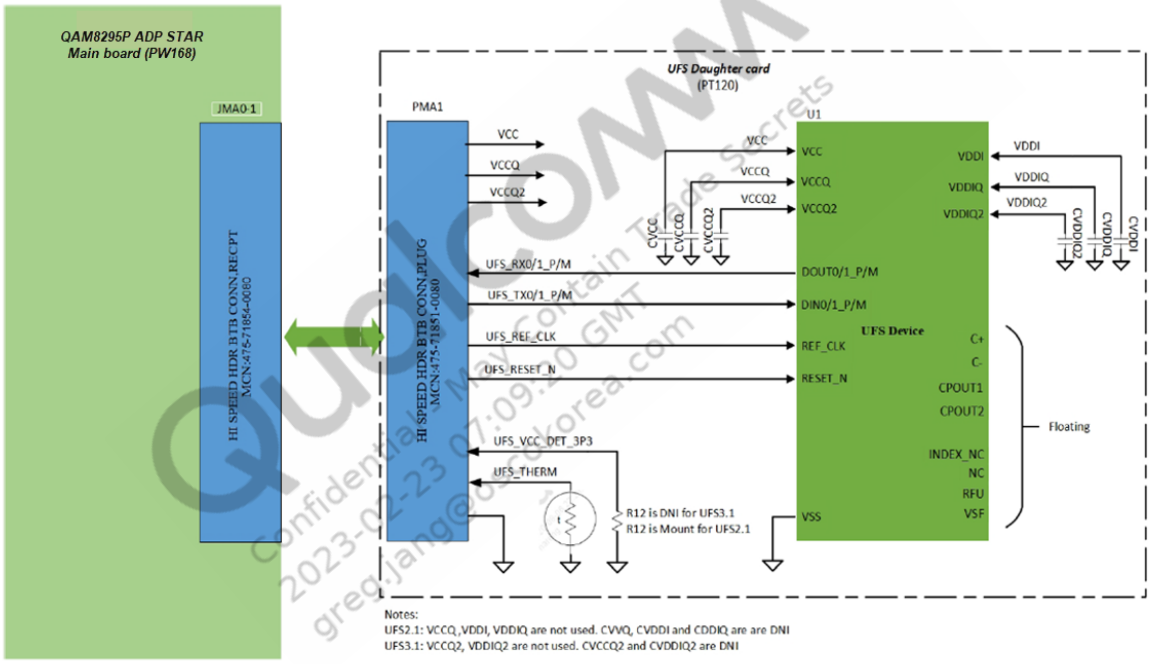


Figure 9-1 UFS memory card block diagram (PT120)