SA8155 Current Consumption Data

80-PE986-7 Rev. C

August 1, 2022

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Revision history

Revision	Date	Description
A	January 2019	Initial release
B	July 2021	Updated Table 4-1 Peak current projection
C	August 2022	Updated STR power projections in Table 4-7 and Table 4-8

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1 Introduction

This document provides current consumption data for SA8155 device. The consumption is highly dependent on software optimization.

This document is intended for engineers and managers who are currently using or are planning to use the SA8155 device.

Information provided in this document is subject to change and comments are provided for informational use only. No commitments are expressed or implied.

1.1 Expectations

Device variation

Current consumption measurements recorded in this document are measured on Qualcomm Technologies, Inc. (QTI) reference hardware and hence may not match current consumption measurements of a customer's design.

Variations in measurement compared to the customer's device can be caused by the SA8155 using different components than the customer design, for example, memory ICs, display ICs, peripheral ICs. Potential variations in measurement compared to an identical SA8155 loaded with identical software are caused by normal silicon process variations in QTI and non-QTI components and power-supply tolerances. Differences in measurement technique, equipment, or temperature also cause variations. Other factors such as floating CMOS inputs or taking measurements at maximum Tx power can affect the reliability and repeatability of current consumption measurements.

Targets and measurements contained here are typical values measured on a specially configured device called ADP-Star resistive current measurement (RCM) evaluation platform. The purpose of this device is to measure power only with 8 GB LPDDR4 memory configuration in a lab bench environment. They are provided as a relative reference point, not as an absolute goal to attain.

Test-case selection

The test cases selected for measurement in this document are intended to provide a wide range of coverage, although the specific conditions a customer need may not appear in this list. There is a test case or combination of test cases that is close enough to the customer requirement to be used for a baseline comparison.

1.2 Customer-platform power optimization

Customer-platform power optimization is best started with comparisons to the QTI platform under one or more baseline test conditions given in this document. After the customer platform and ADP-Star RCM platform are compared and optimized in this known test case, differences between the baseline and required test cases can be measured on the customer platform and analyzed with QTI for optimization, if necessary.

Power optimization of a customer platform is an iterative process that involves the following:

- Identifying power consumption differences between a customer platform and QTI platform in similar test conditions
- Determining the source of those differences, which could be test conditions, hardware-configuration differences, software-control differences, and so on.
- Deciding whether the source is an error that must be corrected or is intentional
- Correcting errors that are identified
- Repeating until all differences are corrected or determined to be intentional

As customers update their hardware platform or integrate new software releases from QTI, power consumption may change, triggering additional power optimization. It is important to understand that during the software development process, current consumption for some test cases may increase, as power improvement features may need to be delayed to a later release to meet stability requirements. Figure 1-1 is a representation of customer power consumption vs. ADP Star power consumption.

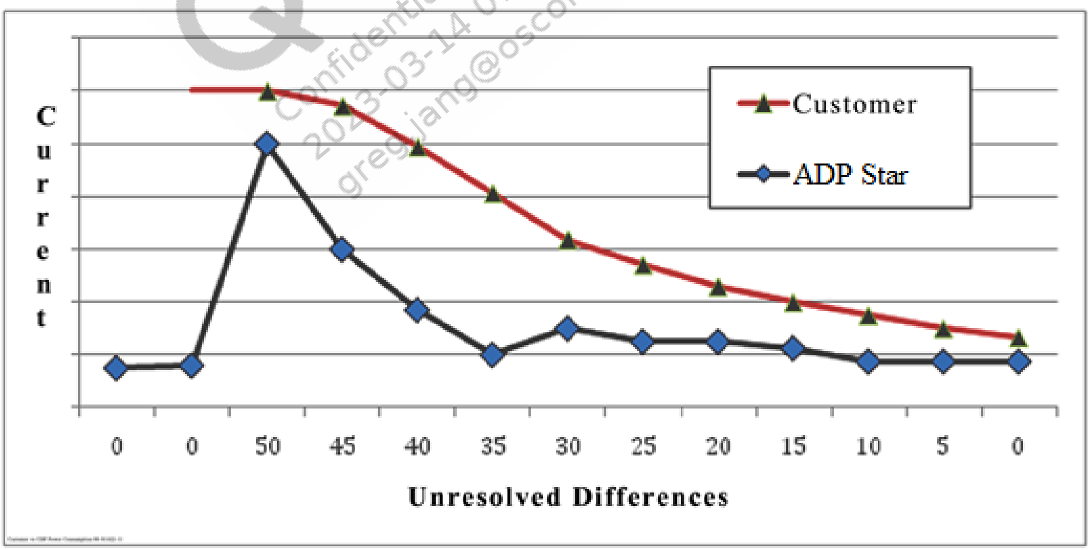

Figure 1-1 Representation of customer vs. ADP Star RCM power consumption

When discussing power optimization requirements with QTI, provide as much information as possible, including the following:

- Specific test conditions
- Available history of power measurements for these test conditions
- Goals for power optimization
- Recent hardware or software changes that may have affected power consumption
- Power consumption breakdown per voltage rail, if possible

1.3 GPIO configuration

To minimize current consumption, OEMs must configure unused GPIOs in one of the following ways:

- As output in their logic low state
- As input with their internal pull-downs enabled

In addition, any GPIO pin configured as an input that is normally driven by a peripheral device (Bluetooth, WLAN, Audio, Display, camera, and so on) must be programmed with an internal pull-down when the corresponding peripheral signal is set to its high-impedance state. The GPIO should then be reprogrammed to remove the pull-down when the peripheral signal is taken out of its high-impedance state.

These steps are required to prevent unwanted oscillation or high current leakage on device pins. For additional information, see *Configuration of Input Pins During Device Sleep* (80-VN499-7).

1.4 Conventions

Function declarations, function names, type declarations, attributes, and code samples appear in a different font, for example, `cp armcc armcpp`.

Code variables appear in angle brackets, for example, `<number>`.

Commands to be entered appear in a different font, for example, **`copy a:*.* b:`**.

Button and key names appear in bold font, for example, click **Save** or press **Enter**.

Shading indicates content that has been added or changed in this revision of the document.

1.5 Technical assistance

For assistance or clarification on information in this document, submit a case to Qualcomm Technologies, Inc. (QTI) at https://createpoint.qti.qualcomm.com/.

If you do not have access to the CDMATech Support website, register for access or send email to support.cdmatech@qti.qualcomm.com.

2 SA8155 energy efficiency benefits

SA8155 uses 7 nm FinFET technology and there is a ~35% of power improvement compared to 14 nm. In addition to 7 nm FinFET technology, there are other IP improvements on SA8155, which enhanced the power efficiency as shown below.

Table 2-1 SA8155 power benefits

IP Improvement areas	Benefits
Next generation Qualcomm® Kryo™ CPU	▪ ~70% reduction in power for gold cores ▪ ~50% reduction in power for silver cores ▪ Operatng Point transition improvements
Next generation Qualcomm® Adreno™ GPU 640	~60% increase in graphics power efficiency
Next generation Qualcomm® Hexagon™ DSP	~20% improvement in power efficiency.
Qualcomm® Universal Bandwidth Compression	More than 30% reduction in bandwidth
Infrastructure improvements	▪ System efficiency and cache architecture optimization (3 MB system cache, and 2 MB L3 cache) ▪ System efficiency improvements with 4 x 16 interfaces, focus on path to DDR power consumption

3 Test setup

Devices used for testing

The following hardware and software configurations are used for the measurements:

- SA8155, PMM8155AU devices are installed on the specially configured device called ADP Star RCM evaluation platform for power measurement purposes only; memory configuration is 8 GB LPDDR4
- Current consumption measurement is performed using QTI power measurement tool on the ADP Star RCM platform. Figure 3-1 depicts the system.
- The following display resolution is used:
  - Two FHD (1920 × 1080), dumb panels,
  - One 4K display connected to native display port
  - Test cases mentioned in this document use different combination of these displays. Some of them use single display and some use multiple displays. Display settings are mentioned in the test cases wherever it is necessary.
- All the test cases described in this document uses SA8155 Premium SKU.

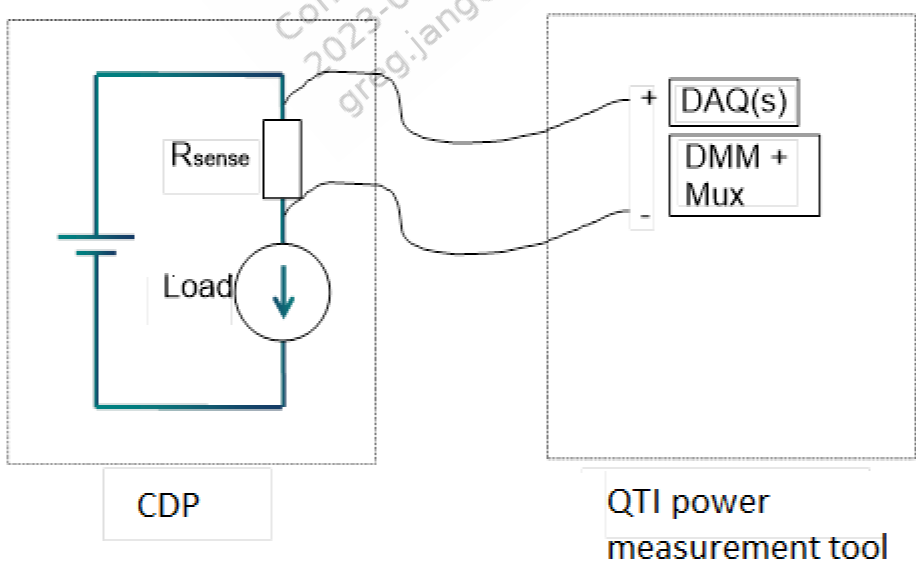

Figure 3-1 ADP Star-SA8155 RCM and QTI power measurement tool

Power tree

See the *SA8155 Power Grid, BOM, and PCB Area Application Note* (80-PE986-17) for the SA8155 chipset's power tree.

Customers are advised to see this document for SA8155 power grid and for the power grid breakdown chart. It shows the power rails for other devices such as the QCA6574A/QCA6595/QCA6696, and external circuitry such as UFS, and SD card. The RCM channel information for the RCM-configured ADP Star is also shown on the power tree.

The current consumption numbers listed in the power tree are estimated worst-case currents. These numbers are preliminary and are intended for PCB routing reference only. In a real-world scenario, all the loads at a node will not run concurrently with peak consumption.

4 Chipset current consumption

Commercial software release target values – Top-level

Commercial software (CS) release target values are predictions of the current consumption for the commercial-quality software release for an operating system. These targets will not be updated after the commercial software has been released.

These values reflect optimized hardware and software configurations. These values are normalized to a 3.3V voltage.

The current or power ranges shown in the following tables are projections/measurements of the current that is expected to be drawn from the power supply during each use case for typical parts (50 percentile).

4.1 Peak power projection (3.3V power supply design)

Customers can use SA8155 peak power projection data for external 3.3V power supply design. Peak power was projected assuming different combinations of following use cases running concurrently using single FHD (1920 × 1080), dumb panel:

- System booting
- CPU benchmark (Geekbench/Quadcore Sax by)
- Camera concurrent use case
- GFX benchmark (Manhattan 3.0)

Table 4-1 Peak current projection

Peak current	Power	Current at 3.3V	Peak Power range*
Peak current at PMIC input (total chipsets including SA8155 + DDR + PMIC)	32 W	9.7 A	1 µs to 1 ms range

*Maximum current is the average of 1 µs to 1 ms range.

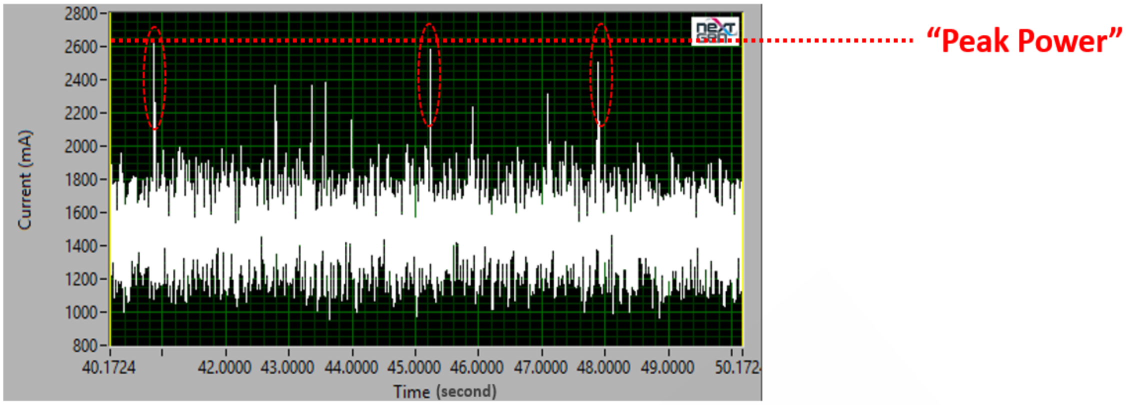

Figure 4-1 Peak power

Peak power is the instantaneous power peak for short durations (1 µs to 1 ms range). This is used to determine the size of a 12 V to -3.3 V power supply in automotive systems.

It is important to understand the power number provided in this section. The power number is meant to reflect peak transient power (uS-mS). It should not be used for thermal analysis where average power provides more meaningful data. See Section 4.2 for thermal analysis.

4.2 Thermal power projection

Thermal power projection assumes a representative LPDDR4 device in the timeframe of SoC production.

NOTE: DDR power consumption depends on DDR vendors and silicon process used. It changes accordingly. QTI recommends that Tier-1 checks the power details from the memory vendors directly. QTI is not responsible for LPDDR4 power changes or updates for individual devices.

4.2.1 Realistic thermal power projection

Multidisplay concurrency use case is designed to simulate real-world use case scenarios for automotive infotainment. Power measurements of these use cases can be used for thermal design.

Multidisplay concurrency use case is defined as follows:

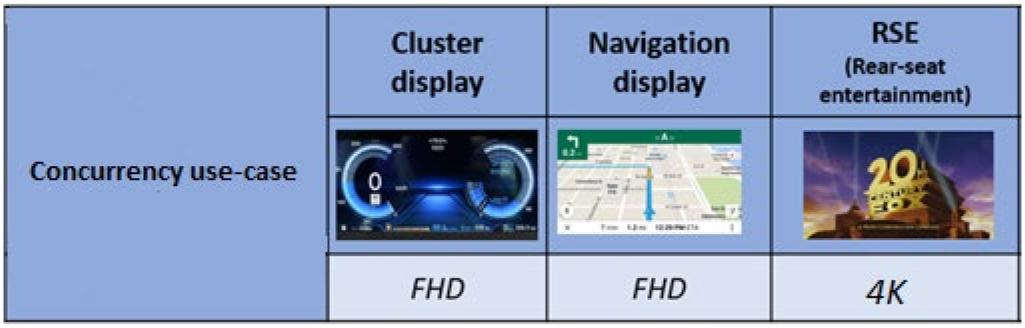

Figure 4-2 Multidisplay concurrency use case

The following table describes the realistic workload on each subsystem CPU (Gold+, Gold and Silver), GPU, and DDR.

Table 4-2 Realistic workload projection

Subsystem	Realistic workload
Gold/Silver CPUs	30% usage: OS, drivers, and applications (cluster, navigation, 4K video playback)
GPU	19% usage: Renderings (cluster, HMI, navigation)
Path-to-DDR (system cache, memory controller, PHY interface)	8% usage: 2.8 GB/sec (out of max 34.1 GB/sec)

Table 4-3 Realistic thermal power projection

Use cases	Realistic thermal power Projection (W)				
Tj	105ºC	85ºC	65ºC	45ºC	25ºC
SA8155 SoC	2.7 W	2.2 W	1.8 W	1.6 W	1.4 W
LPDDR4_1	0.1 W	0.1 W	0.1 W	0.1 W	0.1 W
LPDDR4_2	0.1 W	0.1 W	0.1 W	0.1 W	0.1 W
PMM8155AU_1	0.2 W	0.2 W	0.2 W	0.2 W	0.2 W
PMM8155AU_2	0.5 W	0.3 W	0.3 W	0.2 W	0.2 W
Total (SoC + DDR + PMIC)	3.5 W	2.8 W	2.4 W	2.1 W	1.9 W

PMIC efficiency

SA8155 PMIC efficiency was measured to be between 85% to 87% efficiency at 45ºC, 65ºC and 85ºC depending on the workload.

4.2.2 Worst-case (unrealistic) thermal power projection

The following table describes the assumed use case workload on each subsystem CPU (Gold+, Gold, and Silver), GPU, and DDR.

Table 4-4 Use case workload on subsystem

Subsystem	Maximum workload
Gold/Silver CPUs	90% usage: OS, drivers, applications, connectivity data, fisheye correction, Dhrystone
GPU	90% usage: Renderings (HUD, cluster, HMI, navigation), fisheye correction, Manhattan3.0
Path-to-DDR (system cache, memory controller, PHY interface)	65% usage: 22.2 GB/sec (out of maximum 34.1 GB/sec)

The following table describes the subsystem configurations for above assumed use case (unrealistic) workloads:

Table 4-5 System configuration for worst case (unrealistic use cases)

Subsystem configuration	
Camera (IFE/IPE/CPAS)	Raw data interface (RDI) 2 MP With 5 sensors
Display (SDE)	Compositions: 850 x 480 for HUD 3840 x 2160 for cluster 3840 x 2160 for center stack
Video (VPU)	H.265 encoding (4 x 2 MP x 30 fps)
Audio (LPASS/aDSP)	Voice call via Bluetooth, voice recognition, LEC processing for VR, ANC, in-car communication
cDSP	Image format conversions and VPM for 4 x 2 MP, LDW
NPU	Pedestrian detection
IOs/PHYs	Traffics in PCIe, UFS, USB, CSI, DSI, DisplayPort, WSI, RGMII

The following table is the power breakdown at different temperatures. It is the power projection for the infotainment workload as described above.

Table 4-6 Power breakdown at different temperature for worst case use cases

Use cases	Worst case thermal power Projection (W)		
Tj	85ºC	65ºC	45ºC
SA8155 SoC	11.0 W	10.0 W	9.4 W
LPDDR4_1	0.5 W	0.5 W	0.5 W
LPDDR4_2	0.5 W	0.5 W	0.5 W
PMM8155AU_1	1.0 W	0.9 W	0.8 W
PMM8155AU_2	1.1 W	0.9 W	0.9 W
Total (SoC + DDR + PMIC)	14.0 W	12.7 W	12.0 W

4.3 Low-power modes

Suspend-to-RAM (STR) power projection

STR is the lowest possible power mode for the SA8155 chipset. CPU, GPU, and other subsystems are offline. Current consumed by SA8155 are projected at various temperatures. Since the DDR is in full refresh mode, it draws certain amount of current and it depends on the memory size and vendor of the DDR. A specific representative LPDDR4 device with 4 GB has been used in this projection. This data might change based on the device type, make, and size of the DDR.

Table 4-7 Power projection in different use cases

Use cases	STR power projection			
Tj	85ºC	65ºC	45ºC	25ºC
SoC	79.2 mW	35 mW	15 mW	7 mW
LPDDR4x (x2)	38 mW	22 mW	13 mW	7.5 mW
PMM8155AU (x2)	51.9 mW	25.6 mW	12.9 mW	6 mW
Total	169.1 mW	82.6 mW	40.9 mW	20.5 mW

NOTE: PMIC (PMM8155AU_1) VREG_S4A is always on, even during STR. Therefore it is critical VREG_S4A is not powering any components that need to be powered off during STR.

Partial Array Self-Refresh power projection

Partial array self-refresh (PASR) is a method to self-refresh parts of system memory. When the system is in active state all the regions of memory is refreshed whereas when system in suspend (inactive) state, only used memory is placed in self-refresh mode. Unused parts of memory hierarchy can be turned off when device enters into suspend state.

The aim of PASR is to reduce DRAM power consumption during system suspend state. QTI has integrated PASR solution for automotive to support long duration standby time including weeks.

Table 4-8 STR power projection

Use case	STR power projection			
Tj	85ºC	65ºC	45ºC	25ºC
PASR enabled	TBD	TBD	TBD	TBD
PASR Disabled	169.1 mW	82.6 mW	40.9 mW	20.5 mW

NOTE: See QTI for PASR feature availability.

4.4 Power vs. performance

Following chart projects the SA8155 power consumption of CPU vs. performance.

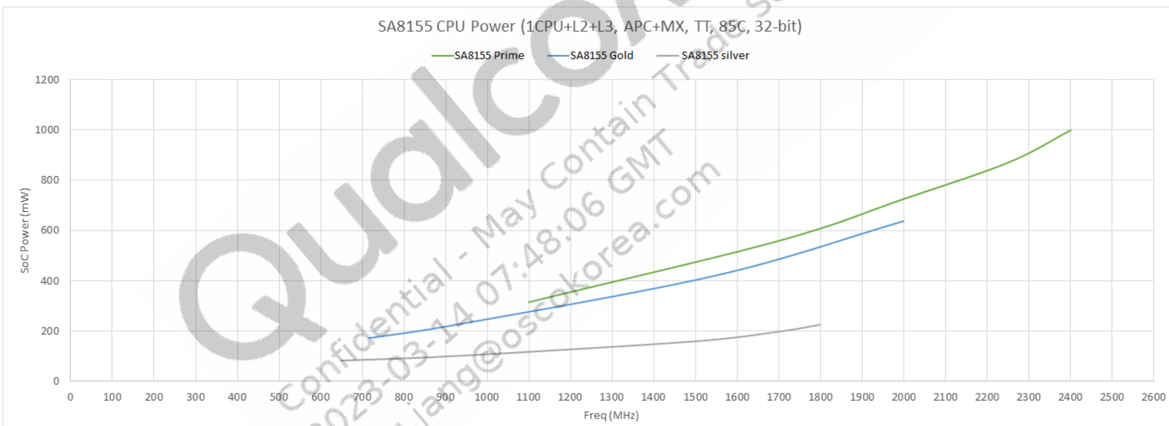

Figure 4-3 SA8155 CPU core power consumption chart

A References

A.1 Related documents

Title	Number
Qualcomm Technologies, Inc.	
SA8155/SA8150/SA8155P/SA8150P Device Specification	80-PE986-1
SA8155 Power Grid, BOM, and PCB Area Application Note	80-PE986-17
SA8155/PMM8155AU/QAM815XP Pin Assignment and GPIO Configuration Spreadsheet	80-PE986-1A
Configuration of Input Pins During Device Sleep	80-VN499-7
SA8155 Hardware Register Description	80-PE986-2X
SA8155/SA8150/SA8155P/SA8150P Device Revision Guide	80-PE986-4
PMM6155AU/PMM8155AU/PMM8195AU Device Specification	80-PE988-1
PMM6155AU/PMM8155AU/PMM8195AU/PMM8540AU/PMM9000AU Power Management IC Design Guidelines	80-PE988-5

A.2 Acronyms and terms

Acronym or term	Definition
CS	Commercial software
DDR	Detailed design review
PASR	Partial array self-refresh
RCM	Resistive current measurement
STR	Suspend to RAM